ATLAS Phase-II Upgrade Project

ATLAS FELIX Phase-II Upgrade: FLX-182 I/O Card Specification

Abstract

This document describes the hardware design of the FLX-182 I/O card, developed as a prototype for the ATLAS Phase-II Readout System.

FELIX Phase-II I/O card hardware specifications		
ATLAS Doc: EDMS Id: EDMS Url:		
Version: Created: Last modified:	1.0 March 3, 2022 May 20, 2025	
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INTRODUCTION

FELIX is a component of the ATLAS Readout System in charge of routing data to and from sub-detector electronics, as well as relaying Timing Trigger and Control (TTC) information to both sub-detector electronics and the downstream DAQ system. Similarly to the Phase-I implementation [1], FELIX consists of custom-made I/O cards hosted by commodity servers equipped with high-speed network interfaces. The requirements for the Phase-II FELIX system are reported in Ref. [2]; specifications are documented in Ref. [3]. The following summarizes the requirements specific to the FELIX I/O card.

- Support for link speeds between 2.56 Gb/s and 25 Gb/s (was 5 Gb/s to 10 Gb/s in Phase-I).
- Adoption of CERN-defined FireFly optical transceivers (MiniPODs in Phase-I).
- Support for 24 links as baseline. The possibility of supporting up to 48 links is not excluded.
- Dedicated optical interface (10 Gb/s uplink, 5 Gb/s downlink) to the Local Trigger Interface (LTI).
- PCIe interface of type Gen4×16 or superior (Gen5×16).
- Presence of electrical ports on the PCIe bracket: JTAG and a sufficient number of connectors for a trigger interface.

This document describes the progress in the design and implementation of the FELIX I/O card. Specifications regarding the overall architecture, interfaces and individual components, as well as considerations on power and cooling are listed in Chapter 2. Next, a FELIX card prototype is presented. FLX-182 is the second Phase-II FELIX card prototype, equipped with an AMD Versal Prime VM1802 FPGA. It supports up to 24 links at 25 Gb/s and the optical LTI interface. The support for TCLink, a technology that ensures picosecond-level phase stability in timing distribution is discussed in Chapter 4. QA/QC tests, including a self-test suite working on FLX-182, are described in Chapter 5. The reliability of the hardware implementation is reviewed in Chapter 6.

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HARDWARE SPECIFICATION

The goal of FELIX is to provide the interface between detector and trigger front-end electronics and the wider ATLAS DAQ system. FELIX is based on commodity server nodes hosting custom-built PCIe I/O cards, with the design of the card common across the entire system. As will be described below, the card is required to support numerous functions and expose multiple different interfaces.

2.1 ARCHITECTURE AND INTERFACES

Specification 2.1 [SPEC-2.1]: *Transceiver Type*

Each Card shall host 'CERN-B' Samtec FireFly transceivers to minimize any decay in optical power across the full operational life-span for systems using VTRx+ front-end transceivers.

Specification 2.2 [SPEC-2.2]: *Transceiver Speed*

Each Card shall use transceivers capable of operating at either up to 10 Gb/s or 25 Gb/s depending on use-case.

Specification 2.3 [SPEC-2.3]: *Number of Optical Links per Card*

Each Card shall host sufficient transceivers to support at least 24 bi-directional links to front-end electronics, alongside a separate bi-directional link to the TTC/BUSY system.

Remark 2.1: *Number of Links per Card*

If possible/required, the number of bi-directional links per card could be greater than 24. This will be continually assessed as component prices and detector requirements evolve.

Specification 2.4 [SPEC-2.4]: *Voltage Protection*

Over/under-voltage protection shall be implemented for every Card.

Specification 2.5 [SPEC-2.5]: *Temperature Protection*

Over-temperature protection shall be implemented on every Card.

Specification 2.6 [SPEC-2.6]: *Component Temperature*

All components must operate in a safe temperature range.

Specification 2.7 [SPEC-2.7]: *Component Lifetimes*

Components chosen for use in FELIX shall have an expected survival lifetime of at least 10 years at normal operating temperatures.

Specification 2.8 [SPEC-2.8]: *External Electrical Interface*

Each Card shall provide a pin for external electrical connections such that, in a lab context, trigger signals can be delivered via this route to cause specific firmware actions to take place.

Specification 2.9 [SPEC-2.9]: *JTAG*

All FPGAs shall be accessible via a standard JTAG interface, accessible via the PCIe bracket.

Specification 2.10 [SPEC-2.10]: *FPGA Configuration from Multiple Images*

By default, FPGA shall load its configuration from a golden image and be able to be switched to an alternate image under software control.

Specification 2.11 [SPEC-2.11]: *Flash Memory*

Each Card shall have sufficient Flash memory to store at least two complete firmware images in a non-volatile manner (i.e. surviving more than 6 months in an unpowered state).

Specification 2.12 [SPEC-2.12]: *I2C*

Each Card shall implement an I2C bus driven peripheral management interface, able to be controlled from the host server via an appropriate interface.

2.2 CLOCKING

The BC clock is received from the LHC and distributed via the Phase-II TTC system. The BC clock frequency is not constant as it evolves during the ramping of the LHC and differs between operation with protons and ions. In addition the clock source can change, leading to sudden jumps in clock phase.

Specification 2.13 [SPEC-2.13]: *BC clock frequency range*

ATLAS systems shall operate in the BC clock frequency range [40.078 MHz – 40.079 MHz].

Remark 2.2: *Need for LHC Clock*

FELIX cards should be able to operate either from the external TTC reference clock or internally generated local clock.

Specification 2.14 [SPEC-2.14]: *LHC BC clock recovery*

FELIX cards should be able to recover the LHC BC clock from the 9.6 Gb/s 8b10b-encoded LTI link.

Specification 2.15 [SPEC-2.15]: *Quality of the received BC clock*

Each ATLAS system shall be responsible for verifying that the quality of the received BC clock (or any multiple of it) meets the criteria for what it will be used and to implement a jitter cleaner if needed (for instance to deliver high-quality clock to FPGAs implementing high-speed serializers).

Specification 2.16 [SPEC-2.16]: *BC clock jitter*

The maximum jitter of the clock shall be that specified in the GBT and/or lpGBT Trigger and Data Link specifications.

2.3 PCB

Specification 2.17 [SPEC-2.17]: *PCB Materials*

PCB for all Modules shall be designed using low-loss and halogen-free materials.

Specification 2.18 [SPEC-2.18]: *Compliance*

All PCB and assembled components shall comply with Technical Coordination and Electronics Coordination requirements and specifications for operating in USA15.

Recommendation 2.1: *Milling*

A mill-down process should be considered if the PCB is thicker than the specifications for the chosen platform technology.

2.3.1 Signal Integrity Constraints

Inductive crosstalk between traces is minimized applying the '3W rule' in both layout and routing. The 3W rule prescribes that traces must be separated by a distance equal to three times the width of a single signal trace, to reduce of possible crosstalk flux of approximately 70%.

Specification 2.19 [SPEC-2.19]: *Impedance for differential traces.*

The impedance of a differential pair is 100 Ω, with the exception of DDR4 module, for which it shall be 95 Ω, and PCIe high-speed trace, for which it shall be 85 Ω.

Specification 2.20 [SPEC-2.20]: *Impedance for single-ended traces.*

The impedance for single-ended traces shall be 50 Ω.

Specification 2.21 [SPEC-2.21]: *Impedance control*

Impedance control is required and shall be within 10% tolerance for both differential and single-ended traces.

Specification 2.22 [SPEC-2.22]: *3W rule for trace separation*

Layout and routing for the PCBs shall follow the 3W rule for trace separation. In addition, the separation distance between signals must be at least three times its distance to the nearby two ground layers.

Specification 2.23 [SPEC-2.23]: *DDR4 signals*

The requirements of the DDR4 layout and routing must be followed.

2.3.2 Layout Design Constraints

Specification 2.24 [SPEC-2.24]: *Vias for high-speed links*

High speed MGT lines shall use as few vertical interconnect access (vias) as possible.

Specification 2.25 [SPEC-2.25]: *Back-drilled vias*

All vias shall be back-drilled if the stub is longer than 0.254 mm (10 mil).

Remark 2.3: *Vias*

In general, high-speed MGT links should have at most four vias per connection.

Recommendation 2.2: *Trace lengths for high-speed links*

The traces of MGT lines should be shorter than 25.4 cm (10 inches).

Recommendation 2.3: *No test points on MGT*

Test points should not be included on the lines carrying multi-Gb/s signals to avoid inducing noise.

2.3.3 Grounding and Shielding

Each signal layer is between two ground layers and all the inner signal paths are implemented as striplines. This arrangement minimizes crosstalk from the other signal layers.

Specification 2.26 [SPEC-2.26]: *Signal layers shall be shielded*

Signal layers shall be between two ground layers.

Recommendation 2.4: *Power layers*

70 µm copper should be used for layers where the current is larger than 50 A. 35 µm copper should be used for the other large-current power layers.

Remark 2.4: *Routing differential signals*

For the differential signals, first design the trace/gap width to match the impedance and then comply the 3W rules for the separation distance pair to pair to reduce the crosstalk and EM interference.

Specification 2.27 [SPEC-2.27]: *Fuses*

Every card shall include fuses to protect the electronics.

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Prototype 2: FLX-182

3.1 Overview

FLX-182 is the second Phase-II FELIX card prototype and is equipped with an AMD Versal Prime VM1802 FPGA. It is PCIe card with full-length, full-height and double width form factor. A fully assembled card is shown in Figure 3.1. The last revision of FLX-182 has been completed in August 2023.

The main features of FLX-182 are:

- 2× PCIe Gen4×8 interface compatible with both PL and CPM4 block;
- Two pairs of 12-link TX/RX of Firefly modules, to support 24 bi-directional optical links at 10 Gb/s or 25 Gb/s;
- One four-link FireFly transceiver (ECUO-B04-28G) for the LTI interface or 100 Gb/s Ethernet;
- One DDR4 Mini-UDIMM;
- Six MMCX electrical connectors on PCIe bracket;
- USB-JTAG and USB-UART interface;
- GbE RJ45 socket;
- Dual-Core Arm Cortex-A72 processing unit.

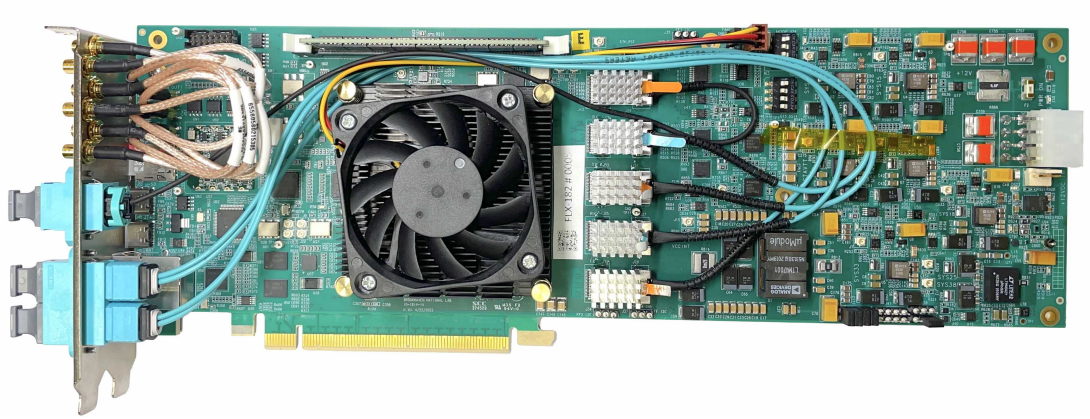

Figure 3.1: Fully assembled FLX-182 prototype card.

3.2 FPGA

3.2.1 AMD Versal Prime VM1802

The FPGA chosen for FLX-182 is AMD Versal Prime XCVM1802-1MSEVSVA2197. The capabilities of VM1802 are reported in Table 3.1 and compared to those of AMD Kintex Ultrascale KU115 used in the Phase-I FLX-712 FELIX card. The device diagram of VM1802 with VSVA2197 package is shown in Figure 3.2 and summarized in Table 3.2. The use of banks in the FLX-182 use-case is illustrated in Figure 3.3. VM1802 is implemented on a single tile, no SLR subdivision is present.

Table 3.1: FPGA resources of FLX-182[4] and Phase-I FLX-712[5] in terms of look-up tables (LUTS), flip-flops (FF), UltraRAM (URAM), block RAM (BRAM) number of transceivers (GTH, GTY), and PCIe generation support.

Resource	VM1802 (FLX-182)	KU115 (FLX-712)
LUTS	899,840	663,360
FF	1,799,680	1,326,720
BRAM [Mb]	34	75.9
URAM [Mb]	130	-
GTY (<32.75 Gb/s)	44	-
GTH (<16.3 Gb/s)	-	64
PCIe interface	$4 \times$ Gen4 $\times 8$	$2 \times$ Gen3 $\times 8$

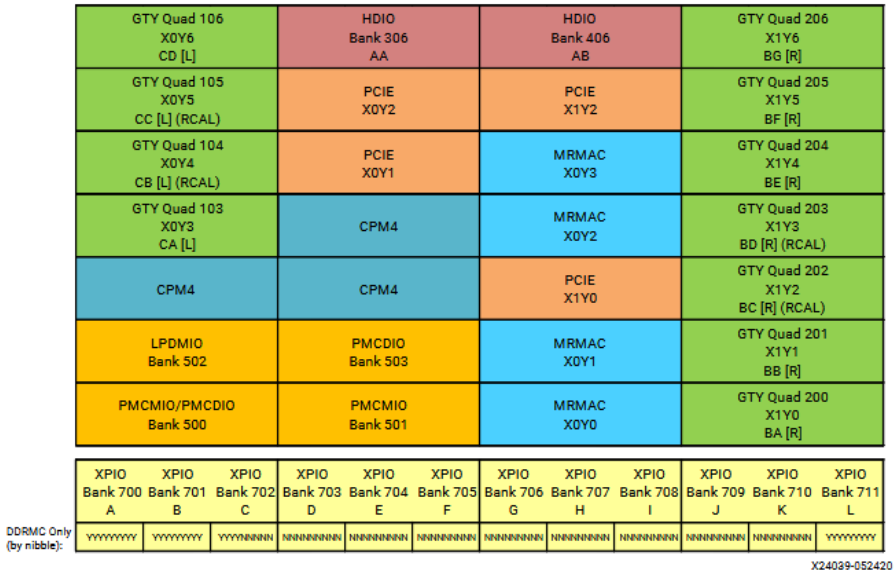

Figure 3.2: Device diagram for VM1802 in VSVA2197 package [6].

Table 3.2: Summary of VM1802 banks.

GTY Banks
11 banks: 200 to 206, 103 to 106
44 x GTY: up to 26.5625 Gb/s
4 x PCIe Gen4 x 8 end-points
IO Banks
12 x High-performance I/O (XPIO) banks: 700 to 711
54 pins / 27 differential pairs per bank
9 x clock capable input pair per bank
2 x High-density I/O (HDIO) banks: 306 and 406
22 pins / 11 differential pairs per bank
2 x clock capable pins per bank
2 x PMC banks: 500 and 501
26 PMC MIO pins per bank (PMC or LPD accessible)
Processing system
FPD (Full Power Domain, dual-core ARM Cortex-A72)
LPD (Low Power Domain, dual-core ARM Cortex-R5F)
1 x LPD bank: bank 502
26 x LPD MIO pins per bank

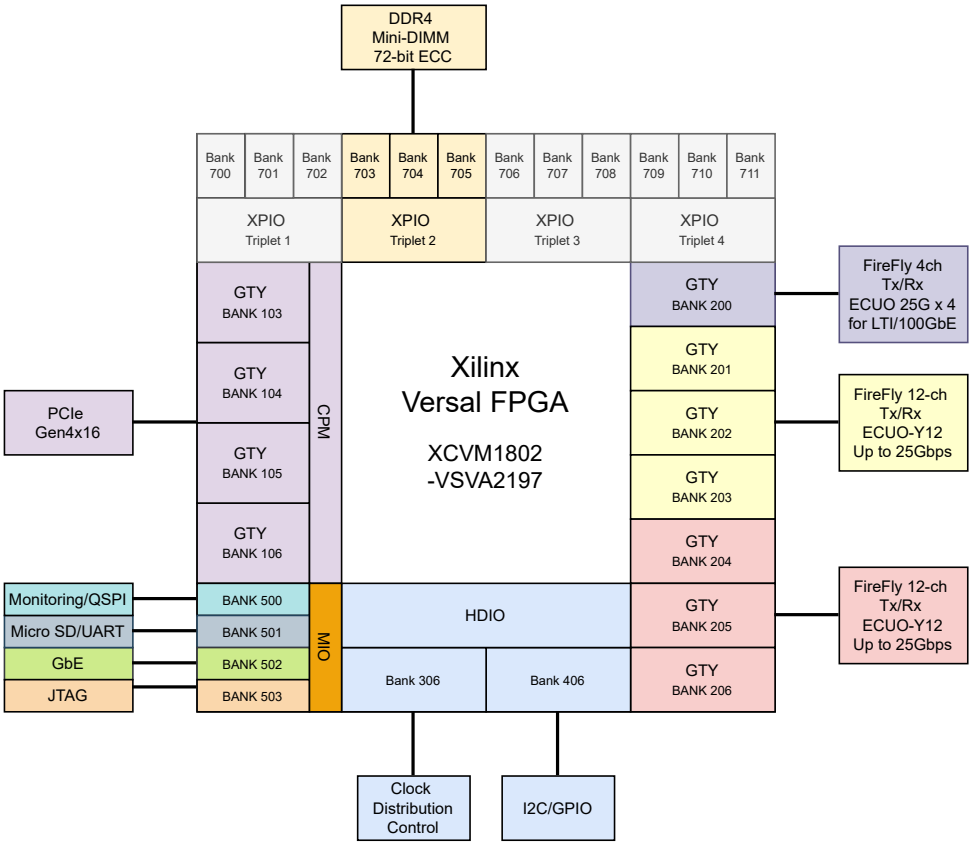

Figure 3.3: Block diagram of FLX-182.

3.2.2 FPGA RESOURCE UTILIZATION

Builds of all firmware flavors have been compiled for FLX-182. As reported in Table 3.3, most flavors are too demanding in terms of FPGA resources. Timing is met only for INTERLAKEN and the same can likely be achieved for FULLMODE and PIXEL. For the remaining flavors the use of the programmable logic basic elements (slices) exceeds 99%. The GBT_SEMISTATIC-2337 variant, already encountered in **??**, implements firmware changes that limit the downlink bandwidth to 1280 Mb/s but reduce the utilization LUTs, FFs and BRAM enough to complete a build. These changes are flavor-independent and could allow for 24-link builds. Nevertheless, the resource utilization of GBT_SEMISTATIC-2337 remains high considering that no headroom is left (above 60% of LUTs utilization routing starts failing) and firmware is likely to evolve. The request for additional firmware features is more likely than shedding of existing ones. In addition, the Readout Team is investigating the implementation of an algorithm [7] that would save CPU use of the readout application in exchange of FPGA resources (mainly BRAM).

Table 3.3: Resource utilization of FELIX Phase-II 24-link firmware flavors on FLX-182. Builds were created from the phase2/master branch in September 2023 using Vivado 2022.2 (https://its.cern.ch/jira/browse/FLX-2292).

Flavor	LUT [%]	FF [%]	BRAM [%]	URAM [%]	WNS [ns]	Notes
GBT_SEMISTATIC	71	52	60	77		Routing failed
FULLMODE	64	41	33	73		2389 failed routes
LPGBT	81	50	76	73		173333 failed routes
PIXEL	62	54	76	73		57263 failed routes
STRIP	88	51	76	93		Routing failed
INTERLAKEN	17	15	33	72	0.00	Timing met
GBT_SEMISTATIC-2337	59	42	41	88	-0.05	Minimal timing violation

3.3 SCHEMATICS

Schematics are available at https://edms.cern.ch/ui/file/2745415/1/felix_ph2_v3_20231207.pdf.

3.4 PCB

3.4.1 DESIGN CONSIDERATIONS

The PCB design follows the Versal ACAP PCB Design User Guide [8] prescriptions to guarantee good signal integrity and meet all requirements.

3.4.1.1 FIREFLY TRANSCEIVERS

The transmit input buffer of FireFly module provides CML-compatible differential inputs presenting a nominal differential input impedance of 100 Ω. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board. The requirement for 25 Gb/s signals layout is critical. To improve signal integrity, no more than two vias on each trace is required. To reduce the stub of via, all traces are on Layer 9 with via L1-10, and Layer 22 with via L1-24. Table 3.4 shows the constraints for traces connected between FPGA GTY and FireFly transceivers for 25 Gb/s signals.

Table 3.4: 25 Gb/s FireFly transceivers trace constraints.

Trace layer	Differential impedance	Intra-pair skew	Max. number of vias	via type
L9, L22	100 Ω	<3 mil	2	L1-10, L1-24

3.4.1.2 PCIE INTERFACE

On FLX-182, FPGA GTY transceivers are connected to PCIe edge directly. Thus, it can support up to PCIe Gen4 x16 lanes by CPM or PL Block PCIe IP in VM1802. The PCB transmission lines could be affected by impedance mismatch, inter-pair skew, intra-pair skew, number of vias on the trace, etc. Some standard values for PCIe standard are listed in Figure 3.4.

Parameter	Value
Frequency	PCIe® Gen 1: 1.25 GHz (2.5 Gbps)
	PCIe® Gen 2: 2.5 GHz (5 Gbps)
	PCIe® Gen 3: 4 GHz (8 Gbps)
	PCIe® Gen 4: 8 GHz (16 Gbps)
AC Coupling Capacitors	AC capacitors required: 75 nF–220 nF
Polarity Reversal	Allowed
Max Intra-Pair Skew	5 mils
Max Inter-Pair Skew	No Inter-pair specification
Trace Impedance	PCIe® Gen 1 and 2:100 Ω ±5% differential; 50 Ω ±5% single ended
	PCIe® Gen 3 and 4: 85 Ω ±5% differential; 42.5 Ω ±5% single ended

Figure 3.4: Parameter of PCIe standard.

The maximum intra-pair skew is restricted to 3 mil. No more than 2 vias are allowed on the high-speed traces. When changing layers, ground vias are placed around the signal vias to provide close route for the return current. To reduce insertion loss, via stubs are kept as minimum as possible. Figure 3.5 illustrates the routing of PCIe high-speed traces. GTY transmitter traces starts from FPGA BGA balls on L1, then go to AC coupling capacitors on L24, then to the PCIe edge. At the GTY receiver side, the signal goes to L22 through L11-24 via, most part of the trace is on L22 until it is underneath of FPGA, then to the BGA ball through L1-24 via.

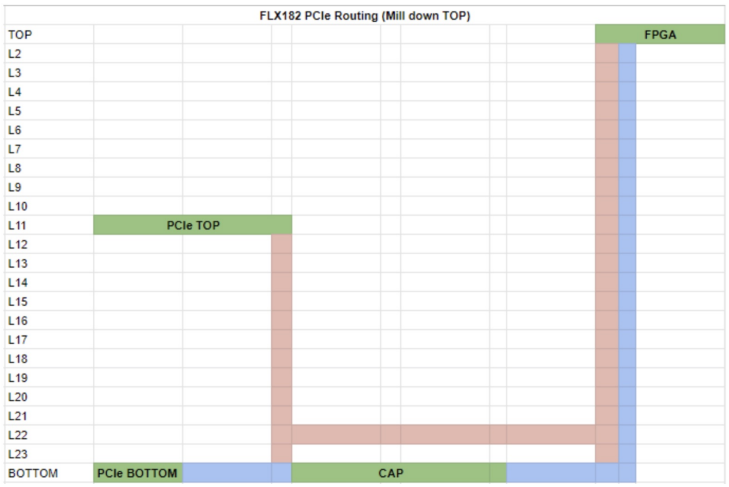

Figure 3.5: Routing layers of PCIe high-speed traces on FLX-182.

3.4.1.3 DDR4

Length control is the most important step for the design of DDR4 with FPGA. Skew constraints for Versal FPGA and DDR4 UDIMM are listed in Table 3.5. Traces are optimized to make the skew as small as possible.

Table 3.5: Skew constraints of DDR4 UDIMM from Ref. [9].

Signal group	Skew constraints [ps]	Skew constraints [mil]
Address to Clock	± 8	± 47
Clock	± 2	± 12
Data to DQS	± 100	± 590
DQS	± 2	± 12
Clock to DQS	± 150	± 885

3.4.2 Stack-up, layout and routing

The 24-layer stack-up used is shown inFigure 3.6. It is composed of three sub-assemblies spanning layers L1-L10, L11-L24, and L1-L24. In total there are 10 signal layers (including Top and Bottom layers), 11 ground layers and 3 dedicated power layers. The overall board thickness is (2.92 ± 0.28) mm. The PCIe gold finger connector uses layers L11 to L24 and its thickness is (1.57 ± 0.13) mm to meet the PCIe specification requirements. The different impedance control for differential traces (85/95/100 Ω) and single-ended traces (50 Ω) is listed in Figure 3.7 for all the signal layers. The PCB fabrication drawing is shown in Figure 3.8 and can be found in high-resolution on EDMS. The dielectric and copper thickness measurements and the impedance measurement report by the manufacturer are included at the end of this subsection. The PCB material is the halogen-free EM890K [10].

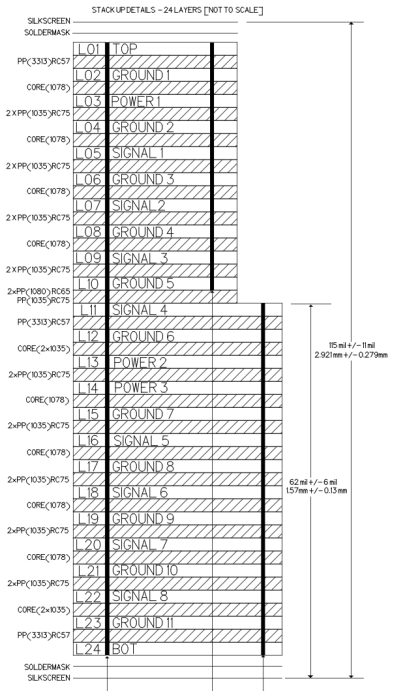

Figure 3.6: PCB stackup for FLX-182.

SCC

Stackup Report

Job Name:000-W24-TJ-101306824-IO-1814-1A-220418TL-230805

Finish Board Thickness(mm):3+/-0.28

Stackup Control Required:

Layer Index	Stackup Buildup	PP Name And RC	Finished Thickness(mm)	Dielectric Thickness(mm)	Dielectric Thickness(Mil/mm)	Finish Cu Thk(oz)	DK(1GHz)	Material Family	Copper Rate(%)
L1	Foil(HTE)		0.04			0.5oz + Plating			31.00
	PP	PP(1080)RC68	0.07	0.073	2.861(0.073)		2.91	EM890K	
L2	HVLP		0.03			1oz			86.00
Core	Core	1*1078	0.076	0.076	2.992(0.076)		2.93	EM890K	
L3	HVLP		0.031			1oz			79
	PP	PP(1035)RC77	0.12	0.123	4.848(0.123)		2.82	EM890K	
	PP	PP(1035)RC77						EM890K	
L4	HVLP		0.03			1oz			86.00
Core	Core	1*1078	0.076	0.076	2.992(0.076)		2.93	EM890K	
L5	HVLP		0.015			0.5oz			54
	PP	PP(1035)RC77	0.13	0.125	4.921(0.125)		2.82	EM890K	
	PP	PP(1035)RC77						EM890K	
L6	HVLP		0.02			0.5oz			86.00
Core	Core	1*1078	0.076	0.076	2.992(0.076)		2.93	EM890K	
L7	HVLP		0.015			0.5oz			13
	PP	PP(1035)RC77	0.12	0.119	4.679(0.119)		2.82	EM890K	
	PP	PP(1035)RC77						EM890K	
L8	HVLP		0.02			0.5oz			86.00
Core	Core	1*1078	0.076	0.076	2.992(0.076)		2.93	EM890K	
L9	HVLP		0.015			0.5oz			43
	PP	PP(1035)RC77	0.13	0.125	4.939(0.125)		2.82	EM890K	
	PP	PP(1035)RC77						EM890K	
L10	Foil(HTE)		0.04			0.5oz + Plating			86.00
	PP	PP(1080)RC68	0.18	0.184	7.240(0.184)		2.88	EM890K	
	PP	PP(1035)RC77						EM890K	
	PP	PP(1080)RC68						EM890K	
L11	Foil(HTE)		0.04			0.5oz + Plating			8.00
	PP	PP(1080)RC68	0.07	0.073	2.873(0.073)		2.91	EM890K	
L12	HVLP		0.03			1oz			87.00
Core	Core	2X1035	0.102	0.102	4.016(0.102)		2.91	EM890K	
L13	HVLP		0.031			1oz			79
	PP	PP(1035)RC77	0.12	0.121	4.751(0.121)		2.82	EM890K	
	PP	PP(1035)RC77						EM890K	
L14	HVLP		0.03			1oz			78.00
Core	Core	1*1078	0.076	0.076	2.992(0.076)		2.93	EM890K	
L15	HVLP		0.031			1oz			86
	PP	PP(1035)RC77	0.12	0.118	4.650(0.118)		2.82	EM890K	
	PP	PP(1035)RC77						EM890K	
L16	HVLP		0.015			0.5oz			23.00
Core	Core	1*1078	0.076	0.076	2.992(0.076)		2.93	EM890K	
L17	HVLP		0.015			0.5oz			86
	PP	PP(1035)RC77	0.12	0.122	4.815(0.122)		2.82	EM890K	
	PP	PP(1035)RC77						EM890K	
L18	HVLP		0.015			0.5oz			36.00
Core	Core	1*1078	0.076	0.076	2.992(0.076)		2.93	EM890K	
L19	HVLP		0.015			0.5oz			86
	PP	PP(1035)RC77	0.12	0.118	4.644(0.118)		2.82	EM890K	
	PP	PP(1035)RC77						EM890K	
L20	HVLP		0.015			0.5oz			7.00
Core	Core	1*1078	0.076	0.076	2.992(0.076)		2.93	EM890K	
L21	HVLP		0.015			0.5oz			87
	PP	PP(1035)RC77	0.12	0.121	4.774(0.121)		2.82	EM890K	
	PP	PP(1035)RC77						EM890K	
L22	HVLP		0.015			0.5oz			28.00
Core	Core	2X1035	0.102	0.102	4.016(0.102)		2.91	EM890K	
L23	HVLP		0.015			0.5oz			86
	PP	PP(1080)RC68	0.08	0.075	2.949(0.075)		2.91	EM890K	
L24	Foil(HTE)		0.04			0.5oz + Plating			39.00

PCIe edge golden finger connector L11-L24 thickness 1.6mm

Impedance Control Required:

Impedance Layer	Impedance Model	Reference Layer	Required Line Width/Spacing(Mil)	Finish Line Width/Spacing(Mil)	Calculated Impedance(Ω)
L1	se_coated_microstrip	L2	7	5.6	50+/-10%
L5	se_stripline	L4/L6	4.3	4.3	50+/-10%
L7	se_stripline	L6/L8	4.3	4.2	50+/-10%
L9	se_stripline	L8/L10	4.3	4.3	50+/-10%
L11	se_stripline	L12/L10	4.3	4	50+/-10%
L16	se_stripline	L17/L15	4.3	4.2	50+/-10%
L18	se_stripline	L19/L17	4.3	4.3	50+/-10%
L20	se_stripline	L21/L19	4.3	4.2	50+/-10%
L22	se_stripline	L23/L21	4.3	5.2	50+/-10%
L24	se_coated_microstrip	L23	7	5.8	50+/-10%
L1	se_coated_microstrip	L2	6	8.9	39+/-5Ω
L5	se_stripline	L4/L6	3.5	6.6	39+/-5Ω
L7	se_stripline	L6/L8	3.5	6.5	39+/-5Ω
L9	se_stripline	L8/L10	3.5	6.6	39+/-5Ω
L11	se_stripline	L12/L10	3.5	6.5	39+/-5Ω
L16	se_stripline	L17/L15	3.5	6.5	39+/-5Ω
L18	se_stripline	L19/L17	3.5	6.6	39+/-5Ω
L20	se_stripline	L21/L19	3.5	6.5	39+/-5Ω
L22	se_stripline	L23/L21	3.5	7.9	39+/-5Ω
L24	se_coated_microstrip	L23	6	9.2	39+/-5Ω
L5	diff_stripline	L4/L6	3.500/3.500	3.700/3.300	95+/-10%
L7	diff_stripline	L6/L8	3.500/3.500	3.700/3.300	95+/-10%
L9	diff_stripline	L8/L10	3.500/3.500	3.700/3.300	95+/-10%
L11	diff_stripline	L12/L10	3.500/3.500	3.000/4.000	95+/-10%
L16	diff_stripline	L17/L15	3.500/3.500	3.700/3.300	95+/-10%
L18	diff_stripline	L19/L17	3.500/3.500	3.700/3.300	95+/-10%
L20	diff_stripline	L21/L19	3.500/3.500	3.700/3.300	95+/-10%
L22	diff_stripline	L23/L21	3.500/3.500	4.100/2.900	95+/-10%
L5	diff_stripline	L4/L6	5.500/4.000	5.100/4.400	85+/-10%
L7	diff_stripline	L6/L8	5.500/4.000	5.100/4.400	85+/-10%
L9	diff_stripline	L8/L10	5.500/4.000	5.100/4.400	85+/-10%
L11	diff_stripline	L12/L10	5.500/4.000	4.500/5.000	85+/-10%
L16	diff_stripline	L17/L15	5.500/4.000	5.100/4.400	85+/-10%
L18	diff_stripline	L19/L17	5.500/4.000	5.100/4.400	85+/-10%
L20	diff_stripline	L21/L19	5.500/4.000	5.100/4.400	85+/-10%
L22	diff_stripline	L23/L21	5.500/4.000	5.700/3.800	85+/-10%
L24	diff_coated_microstrip	L23	5.400/4.000	5.300/4.100	85+/-10%
L5	diff_stripline	L4/L6	3.700/4.300	3.700/4.300	100+/-10%
L7	diff_stripline	L6/L8	3.700/4.300	3.700/4.300	100+/-10%
L9	diff_stripline	L8/L10	3.700/4.300	3.700/4.300	100+/-10%
L11	diff_stripline	L12/L10	3.700/4.300	3.000/5.000	100+/-10%
L16	diff_stripline	L17/L15	3.700/4.300	3.600/4.400	100+/-10%
L18	diff_stripline	L19/L17	3.700/4.300	3.700/4.300	100+/-10%
L20	diff_stripline	L21/L19	3.700/4.300	3.600/4.400	100+/-10%
L22	diff_stripline	L23/L21	3.700/4.300	4.100/3.900	100+/-10%

Figure 3.7: Stackup and impedance control table for the FLX-182.

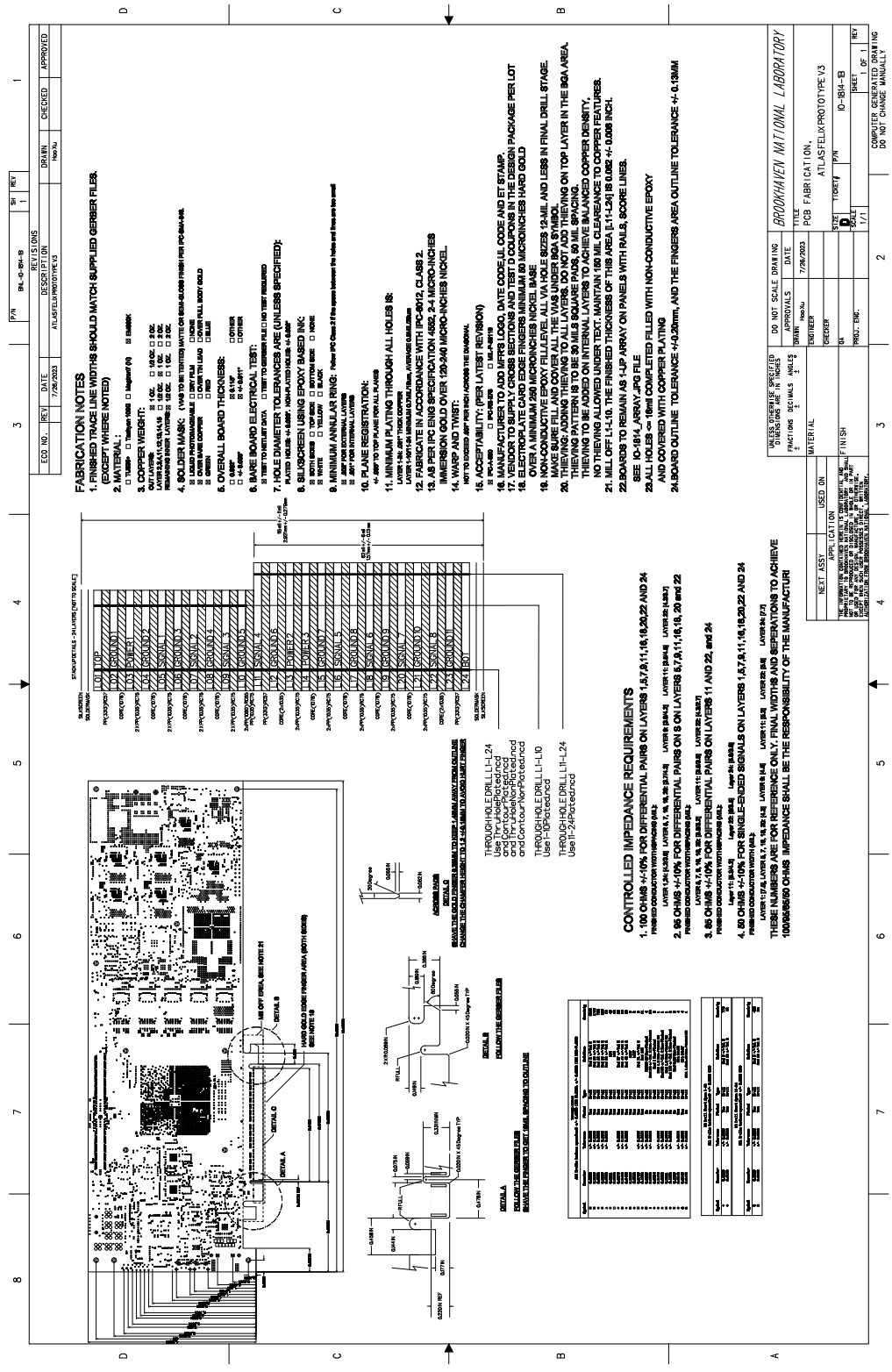

Figure 3.8: Fabrication drawing for FLX-182.

SCC

介 质 层 厚 度 试 验 报 告

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DIELECTRIC THICKNESS TEEPORT

NO.: 36.23 R 1PL-06.05-1 A

客 户 Customer	Shennan Circuits USA, Inc	档案号 File No.	101422538	生产号 Product No.	11-101338267-1-01-000
零件号 Part No.	IO-1814-1B PCB	样品数 Sample Size	1	日 期 Date	2023-11-3

介 质 层 厚 度（单 位： 微 米）

Dielectric Thickness （Unit：μm)

层 数 Layer	要 求 厚 度 Requirement	实际测量值 result	层 数 Layer	要 求 厚 度 Requirement	实际测量值 result
L1-L2	86 ± 18	90.8			
L2-L3	76 ± 18	75.4			
L3-L4	119 ± 18	118.5			
L4-L5	76 ± 18	76.9			
L5-L6	122 ± 25	116.9			
L6-L7	76 ± 18	76.9			
L7-L8	116 ± 18	115.4			
L8-L9	76 ± 18	73.8			
L9-L10	123 ± 25	124.6			
L10-L11	214 ± 38	218.5			
L11-L12	87 ± 18	90.8			
L12-L13	102 ± 18	95.4			
L13-L14	118 ± 18	116.9			
L14-L15	76 ± 18	81.5			
L15-L16	116 ± 18	115.4			
L16-L17	76 ± 18	73.8			
L17-L18	120 ± 25	113.8			
L18-L19	76 ± 18	76.9			
L19-L20	116 ± 18	118.5			
L20-L21	76 ± 18	80.0			
L21-L22	119 ± 18	121.5			
L22-L23	102 ± 18	104.6			
L23-L24	90 ± 18	92.3			

结 论： √ 合 格 ☐ 不 合 格

Final Disposition Accept Reject

试验者： 雷淑钧 审 核： 阮文桂

Tester Approved by

SCC

各 层 铜 厚 试 验 报 告

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COPPER THICKNESS TEST REPORT

NO.： 36.23 R PL-58-A

客 户 Customer	Shennan Circuits USA, Inc	档案号 File No.	101422538	生产号 Product No.	11-101338267-1-01-000
零件号 Part No.	IO-1814-1B PCB	样品数 Sample Size	1	日 期 Date	2023-11-3

各层铜厚度（单位： 微米）
Corper Thickness （Unit：μm)

层 数 Layer	要 求 厚 度 Requirement	实际测量值 Result	层 数 Layer	要 求 厚 度 Requirement	实际测量值 Result
L1	≥30	48.5			
L2	≥1oz	31.5			
L3	≥1oz	33.8			
L4	≥1oz	33.1			
L5	≥0.5oz	16.2			
L6	≥0.5oz	19.2			
L7	≥0.5oz	17.7			
L8	≥0.5oz	17.7			
L9	≥0.5oz	20.8			
L10	≥1oz	41.5			
L11	≥1oz	33.1			
L12	≥1oz	33.1			
L13	≥1oz	33.1			
L14	≥1oz	33.8			
L15	≥1oz	33.8			
L16	≥0.5oz	14.6			
L17	≥0.5oz	19.2			
L18	≥0.5oz	16.9			
L19	≥0.5oz	16.2			
L20	≥0.5oz	19.2			
L21	≥0.5oz	16.2			
L22	≥0.5oz	14.6			
L23	≥0.5oz	13.8			
L24	≥30	45.4			

结 论： Final Disposition	√ 合 格 Accept	☐ 不合格 Reject
试验者： Tester 雷淑钧	审 核： Approved by	阮文桂

Impedance Measurement Record

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物资编码/Material Coding: 101422538 零件号/Part No: IO-1814-1B PCB

生产号/Product No: 11-101338267-1-01-000 日期/Date: 2023-9-23

操作人/Operator: 雷淑钧 审核人/Emendator: 阮文桂

NO.	Description	SPEC	Line Width	+	-	Average	Result	Operator	Date
1	L1	50	7.20	10%	10%	54.84	PASS	YCJ	2023-9-23
1	L5	50	4.40	10%	10%	51.34	PASS	YCJ	2023-9-23
1	L7	50	4.30	10%	10%	53.00	PASS	YCJ	2023-9-23
1	L9	50	4.40	10%	10%	51.10	PASS	YCJ	2023-9-23
1	L11	50	5.30	10%	10%	53.55	PASS	YCJ	2023-9-23
1	L16	50	4.30	10%	10%	51.97	PASS	YCJ	2023-9-23
1	L18	50	4.30	10%	10%	52.86	PASS	YCJ	2023-9-23
1	L20	50	4.30	10%	10%	52.42	PASS	YCJ	2023-9-23
1	L22	50	5.40	10%	10%	51.81	PASS	YCJ	2023-9-23
1	L24	50	7.60	10%	10%	49.38	PASS	YCJ	2023-9-23
1	L1	100	4.00/4.00	10%	10%	108.56	PASS	YCJ	2023-9-23
1	L5	95	3.80/3.20	10%	10%	98.53	PASS	YCJ	2023-9-23
1	L5	100	3.80/4.20	10%	10%	100.38	PASS	YCJ	2023-9-23
1	L7	95	3.80/3.20	10%	10%	97.58	PASS	YCJ	2023-9-23
1	L7	100	3.70/4.30	10%	10%	101.58	PASS	YCJ	2023-9-23
1	L9	100	3.80/4.20	10%	10%	99.28	PASS	YCJ	2023-9-23
1	L11	85	5.90/3.60	10%	10%	78.27	PASS	YCJ	2023-9-23
1	L11	95	3.55/3.45	10%	10%	97.97	PASS	YCJ	2023-9-23
1	L11	100	3.55/4.45	10%	10%	109.40	PASS	YCJ	2023-9-23
1	L16	95	3.80/3.20	10%	10%	95.90	PASS	YCJ	2023-9-23
1	L16	100	3.70/4.30	10%	10%	102.66	PASS	YCJ	2023-9-23
1	L18	100	3.80/4.20	10%	10%	100.21	PASS	YCJ	2023-9-23
1	L20	95	3.80/3.20	10%	10%	94.10	PASS	YCJ	2023-9-23
1	L20	100	3.70/4.30	10%	10%	100.08	PASS	YCJ	2023-9-23
1	L22	85	5.90/3.60	10%	10%	85.93	PASS	YCJ	2023-9-23
1	L22	95	4.25/2.75	10%	10%	94.38	PASS	YCJ	2023-9-23
1	L22	100	4.25/3.75	10%	10%	98.63	PASS	YCJ	2023-9-23
1	L24	85	5.90/3.50	10%	10%	86.22	PASS	YCJ	2023-9-23
1	L24	100	4.10/3.90	10%	10%	97.64	PASS	YCJ	2023-9-23
2	L1	50	7.20	10%	10%	54.38	PASS	YCJ	2023-9-23
2	L5	50	4.40	10%	10%	53.03	PASS	YCJ	2023-9-23
2	L7	50	4.30	10%	10%	52.62	PASS	YCJ	2023-9-23
2	L9	50	4.40	10%	10%	50.42	PASS	YCJ	2023-9-23
2	L11	50	5.30	10%	10%	53.78	PASS	YCJ	2023-9-23
2	L16	50	4.30	10%	10%	52.42	PASS	YCJ	2023-9-23
2	L18	50	4.30	10%	10%	53.03	PASS	YCJ	2023-9-23
2	L20	50	4.30	10%	10%	53.57	PASS	YCJ	2023-9-23
2	L22	50	5.40	10%	10%	50.87	PASS	YCJ	2023-9-23
2	L24	50	7.60	10%	10%	50.26	PASS	YCJ	2023-9-23
2	L1	100	4.00/4.00	10%	10%	101.45	PASS	YCJ	2023-9-23
2	L5	95	3.80/3.20	10%	10%	98.91	PASS	YCJ	2023-9-23
2	L5	100	3.80/4.20	10%	10%	100.66	PASS	YCJ	2023-9-23
2	L7	95	3.80/3.20	10%	10%	98.01	PASS	YCJ	2023-9-23
2	L7	100	3.70/4.30	10%	10%	100.46	PASS	YCJ	2023-9-23
2	L9	100	3.80/4.20	10%	10%	99.47	PASS	YCJ	2023-9-23
2	L11	85	5.90/3.60	10%	10%	79.50	PASS	YCJ	2023-9-23
2	L11	95	3.55/3.45	10%	10%	102.76	PASS	YCJ	2023-9-23
2	L11	100	3.55/4.45	10%	10%	101.85	PASS	YCJ	2023-9-23
2	L16	95	3.80/3.20	10%	10%	95.95	PASS	YCJ	2023-9-23
2	L16	100	3.70/4.30	10%	10%	101.84	PASS	YCJ	2023-9-23
2	L18	100	3.80/4.20	10%	10%	100.65	PASS	YCJ	2023-9-23
2	L20	95	3.80/3.20	10%	10%	96.16	PASS	YCJ	2023-9-23
2	L20	100	3.70/4.30	10%	10%	100.65	PASS	YCJ	2023-9-23
2	L22	85	5.90/3.60	10%	10%	85.44	PASS	YCJ	2023-9-23

2	L22	95	4.25/2.75	10%	10%	94.40	PASS	YCJ	2023-9-23
2	L22	100	4.25/3.75	10%	10%	98.55	PASS	YCJ	2023-9-23
2	L24	85	5.90/3.50	10%	10%	86.12	PASS	YCJ	2023-9-23
2	L24	100	4.10/3.90	10%	10%	99.52	PASS	YCJ	2023-9-23
3	L1	50	7.20	10%	10%	50.87	PASS	YCJ	2023-9-23
3	L5	50	4.40	10%	10%	54.15	PASS	YCJ	2023-9-23
3	L7	50	4.30	10%	10%	51.28	PASS	YCJ	2023-9-23
3	L9	50	4.40	10%	10%	51.47	PASS	YCJ	2023-9-23
3	L11	50	5.30	10%	10%	53.03	PASS	YCJ	2023-9-23
3	L16	50	4.30	10%	10%	53.07	PASS	YCJ	2023-9-23
3	L18	50	4.30	10%	10%	53.37	PASS	YCJ	2023-9-23
3	L20	50	4.30	10%	10%	51.61	PASS	YCJ	2023-9-23
3	L22	50	5.40	10%	10%	50.89	PASS	YCJ	2023-9-23
3	L24	50	7.60	10%	10%	54.98	PASS	YCJ	2023-9-23
3	L1	100	4.00/4.00	10%	10%	99.69	PASS	YCJ	2023-9-23
3	L5	95	3.80/3.20	10%	10%	98.87	PASS	YCJ	2023-9-23
3	L5	100	3.80/4.20	10%	10%	100.61	PASS	YCJ	2023-9-23
3	L7	95	3.80/3.20	10%	10%	96.54	PASS	YCJ	2023-9-23
3	L7	100	3.70/4.30	10%	10%	101.13	PASS	YCJ	2023-9-23
3	L9	100	3.80/4.20	10%	10%	100.45	PASS	YCJ	2023-9-23
3	L11	85	5.90/3.60	10%	10%	77.28	PASS	YCJ	2023-9-23
3	L11	95	3.55/3.45	10%	10%	97.18	PASS	YCJ	2023-9-23
3	L11	100	3.55/4.45	10%	10%	104.75	PASS	YCJ	2023-9-23
3	L16	95	3.80/3.20	10%	10%	96.14	PASS	YCJ	2023-9-23
3	L16	100	3.70/4.30	10%	10%	102.25	PASS	YCJ	2023-9-23
3	L18	100	3.80/4.20	10%	10%	101.50	PASS	YCJ	2023-9-23
3	L20	95	3.80/3.20	10%	10%	93.02	PASS	YCJ	2023-9-23
3	L20	100	3.70/4.30	10%	10%	100.03	PASS	YCJ	2023-9-23
3	L22	85	5.90/3.60	10%	10%	85.38	PASS	YCJ	2023-9-23
3	L22	95	4.25/2.75	10%	10%	95.48	PASS	YCJ	2023-9-23
3	L22	100	4.25/3.75	10%	10%	98.26	PASS	YCJ	2023-9-23
3	L24	85	5.90/3.50	10%	10%	84.02	PASS	YCJ	2023-9-23
3	L24	100	4.10/3.90	10%	10%	99.00	PASS	YCJ	2023-9-23
4	L1	50	7.20	10%	10%	54.54	PASS	YCJ	2023-9-23
4	L5	50	4.40	10%	10%	51.45	PASS	YCJ	2023-9-23
4	L7	50	4.30	10%	10%	52.04	PASS	YCJ	2023-9-23
4	L9	50	4.40	10%	10%	51.00	PASS	YCJ	2023-9-23
4	L11	50	5.30	10%	10%	51.70	PASS	YCJ	2023-9-23
4	L16	50	4.30	10%	10%	51.87	PASS	YCJ	2023-9-23
4	L18	50	4.30	10%	10%	51.32	PASS	YCJ	2023-9-23
4	L20	50	4.30	10%	10%	51.46	PASS	YCJ	2023-9-23
4	L22	50	5.40	10%	10%	50.41	PASS	YCJ	2023-9-23
4	L24	50	7.60	10%	10%	53.17	PASS	YCJ	2023-9-23
4	L1	100	4.00/4.00	10%	10%	102.32	PASS	YCJ	2023-9-23
4	L5	95	3.80/3.20	10%	10%	98.37	PASS	YCJ	2023-9-23
4	L5	100	3.80/4.20	10%	10%	101.14	PASS	YCJ	2023-9-23
4	L7	95	3.80/3.20	10%	10%	96.87	PASS	YCJ	2023-9-23
4	L7	100	3.70/4.30	10%	10%	101.29	PASS	YCJ	2023-9-23
4	L9	100	3.80/4.20	10%	10%	99.79	PASS	YCJ	2023-9-23
4	L11	85	5.90/3.60	10%	10%	86.38	PASS	YCJ	2023-9-23
4	L11	95	3.55/3.45	10%	10%	94.81	PASS	YCJ	2023-9-23
4	L11	100	3.55/4.45	10%	10%	105.44	PASS	YCJ	2023-9-23
4	L16	95	3.80/3.20	10%	10%	97.70	PASS	YCJ	2023-9-23
4	L16	100	3.70/4.30	10%	10%	101.58	PASS	YCJ	2023-9-23
4	L18	100	3.80/4.20	10%	10%	100.24	PASS	YCJ	2023-9-23
4	L20	95	3.80/3.20	10%	10%	95.23	PASS	YCJ	2023-9-23
4	L20	100	3.70/4.30	10%	10%	100.16	PASS	YCJ	2023-9-23
4	L22	85	5.90/3.60	10%	10%	85.07	PASS	YCJ	2023-9-23
4	L22	95	4.25/2.75	10%	10%	94.72	PASS	YCJ	2023-9-23
4	L22	100	4.25/3.75	10%	10%	97.41	PASS	YCJ	2023-9-23
4	L24	85	5.90/3.50	10%	10%	84.38	PASS	YCJ	2023-9-23
4	L24	100	4.10/3.90	10%	10%	106.98	PASS	YCJ	2023-9-23
5	L1	50	7.20	10%	10%	49.18	PASS	YCJ	2023-9-23
5	L5	50	4.40	10%	10%	52.28	PASS	YCJ	2023-9-23
5	L7	50	4.30	10%	10%	51.67	PASS	YCJ	2023-9-23

5	L9	50	4.40	10%	10%	52.88	PASS	YCJ	2023-9-23
5	L11	50	5.30	10%	10%	52.00	PASS	YCJ	2023-9-23
5	L16	50	4.30	10%	10%	52.44	PASS	YCJ	2023-9-23
5	L18	50	4.30	10%	10%	50.79	PASS	YCJ	2023-9-23
5	L20	50	4.30	10%	10%	51.19	PASS	YCJ	2023-9-23
5	L22	50	5.40	10%	10%	51.19	PASS	YCJ	2023-9-23
5	L24	50	7.60	10%	10%	54.99	PASS	YCJ	2023-9-23
5	L1	100	4.00/4.00	10%	10%	101.67	PASS	YCJ	2023-9-23
5	L5	95	3.80/3.20	10%	10%	98.27	PASS	YCJ	2023-9-23
5	L5	100	3.80/4.20	10%	10%	100.26	PASS	YCJ	2023-9-23
5	L7	95	3.80/3.20	10%	10%	97.63	PASS	YCJ	2023-9-23
5	L7	100	3.70/4.30	10%	10%	99.55	PASS	YCJ	2023-9-23
5	L9	100	3.80/4.20	10%	10%	100.08	PASS	YCJ	2023-9-23
5	L11	85	5.90/3.60	10%	10%	77.32	PASS	YCJ	2023-9-23
5	L11	95	3.55/3.45	10%	10%	93.27	PASS	YCJ	2023-9-23
5	L11	100	3.55/4.45	10%	10%	107.01	PASS	YCJ	2023-9-23
5	L16	95	3.80/3.20	10%	10%	97.08	PASS	YCJ	2023-9-23
5	L16	100	3.70/4.30	10%	10%	102.02	PASS	YCJ	2023-9-23
5	L18	100	3.80/4.20	10%	10%	98.56	PASS	YCJ	2023-9-23
5	L20	95	3.80/3.20	10%	10%	94.16	PASS	YCJ	2023-9-23
5	L20	100	3.70/4.30	10%	10%	99.81	PASS	YCJ	2023-9-23
5	L22	85	5.90/3.60	10%	10%	85.07	PASS	YCJ	2023-9-23
5	L22	95	4.25/2.75	10%	10%	94.29	PASS	YCJ	2023-9-23
5	L22	100	4.25/3.75	10%	10%	98.21	PASS	YCJ	2023-9-23
5	L24	85	5.90/3.50	10%	10%	86.89	PASS	YCJ	2023-9-23
5	L24	100	4.10/3.90	10%	10%	98.01	PASS	YCJ	2023-9-23

3.4.3 CERTIFICATION

PCB fabrication requires a number of certifications of compliance and inspection. The ones that will be provided are the Certification of Compliance IPC-6012 Class-2/IPC-600 Class-2, the Electrical Test Certification of Compliance, Final Audit Report, Dielectric Thickness Test Report, Micro-cross Section Report, and impedance Test Report. All of the above certificates for FLX-182 will be included in Appendix once they become available. IPC [11] – Association Connecting Electronics Industries – provides standards for the production and assembly of electronics and are used worldwide. The IPC-6012 Class-2 Certification is the Qualification and Performance Specification for Rigid Printed Boards provided by IPC. IPC-6012 establishes and defines the qualification and performance requirements for the fabrication of rigid printed boards. The IPC-A-600 Certificate for Acceptability of Printed Boards Training and Certification program is applied.

3.5 Power scheme

3.5.1 FPGA power consumption

The Xilinx XPE tool version 2021.2 is used to estimate the power consumption of the VM1802 FPGA. The power consumption for seven different configurations is presented in Table 3.6 and used for the power distribution and heat dissipation design. A screenshot of the XPE estimate is shown in Figure 3.9.

The per-rail power estimated by XPE is summarized in Figure 3.10. The FPGA power consumption scenarios considered for the hardware design are rather conservative with respect to the FELIX use case. In fact, FELIX firmware does not use clocks with frequency higher than 250 MHz [12]. The power consumption reported by Vivado for the firmware builds presented in Table 3.3 is reported in Table 3.7 and does not exceed 40 W.

Table 3.6: Parameters used in the Xilinx XPE tool to estimate the power for the Xilinx Versal VM1802 FPGA. The uncertainty on these power estimates is 15%.

Case	GTY	Logic	Clock (MHz)	Toggle Rate	Power (W)
1	44	70%	320	12.5%	63
2	44	70%	320	25.0%	76
3	44	70%	320 & 100	25.0%	56
4	44	80%	320	12.5%	65
5	44	80%	320	25.0%	79
6	44	90%	320	12.5%	69
7	44	90%	320	25.0%	85

Table 3.7: FPGA power consumption reported by firmware builds with FELIX Vivado 2022.2. https://its.cern.ch/jira/browse/FLX-2292.

Firmware flavor	Power (W)
GBT_SEMISTATIC	29
FULLMODE	32
LPGBT	34
PIXEL	33
STRIPS	33
INTERLAKEN	35

3.5.2 Power distribution

A breakdown of power rails currents is listed in Table 3.8, the power scheme, including component efficiency and power-on sequence, is shown in Table 3.9.

A low noise DC/DC LTM4700 [13] regulator is used for 0.8 V power rail. LTM4700 can provide up to 100 A current with small ripple. LTM4642 [14] DC/DC regulator is used for the 3.8 V and 2.5 V rails used to feed the MGTYVCCAUX 1.5 V rail. The LTM4638 [15] step-down regulator is used for the remaining power rails. This component can output up to 15 A, guaranteeing sizeable headroom. The total power consumption is ~ 96.6 W. Power is supplied to the card via one 8-pin PCIe power connector rated for 150 W. No power is drawn from the 12 V pins of the PCIe slot by design, to avoid high current flow in the host motherboard.

The power management will implement power-on control and monitoring of current, voltage, and power module temperature. An ADM1266 sequencer [16] controls the power-on sequence by setting the RUN signal of each power rail. The configuration of ADM1266 is programmed into the EEPROM on the chip. Thus, the configuration is loaded from the EEPROM directly after 12 V input is on. The 12 V input and other power

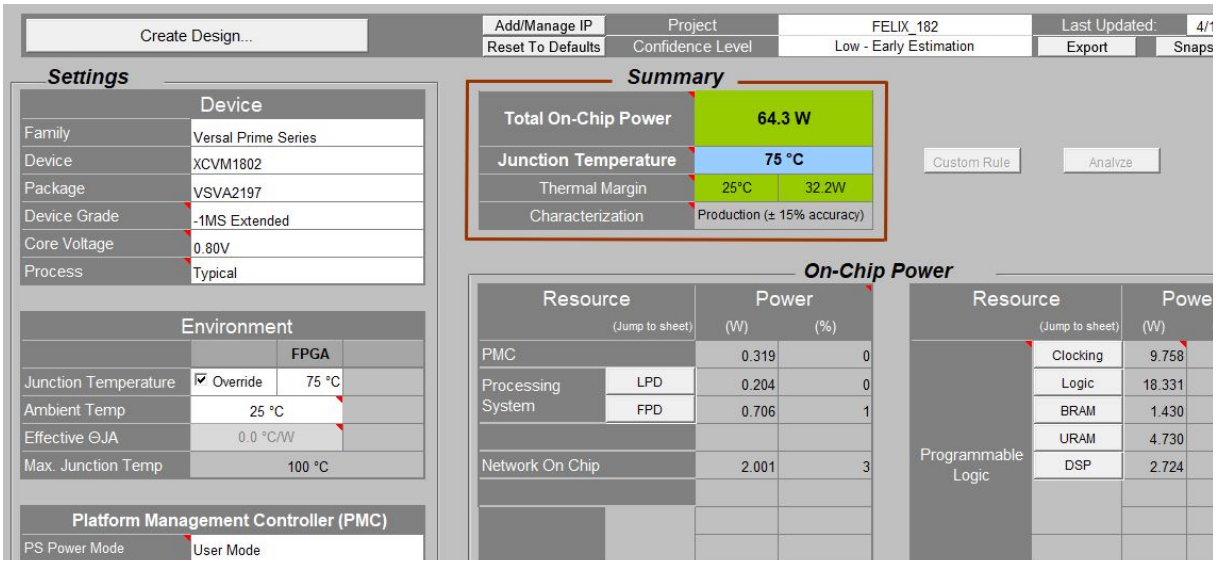


Figure 3.9: Xilinx Power Estimator spreadsheet for a VM1802 FPGA.

Platform Management Controller (PMC)						Current Requirements				
		Supply	Voltage (V)	oltage Range (V	Step Load %	Static (A)	Dynamic (A)	Total (A)	wer-On Current	Power Rail Group
		VCC_PMC	0.8	0.775 - 0.825	33%	0.005	0.147	0.152	-	0V80 (Digital)
		VCCO_503	1.8V	1.710 - 1.890	100%	0	0.004	0.004	-	1V8_VCCO (Digital)
		VCCO_500	1.8V	1.710 - 1.890	100%	0	0.007	0.007	-	1V8_VCCO (Digital)
		VCCO_501	1.8V	1.710 - 1.890	100%	0	0	0	-	1V8_VCCO (Digital)
		VCCAUX_PMC	1.5	1.455 - 1.545	100%	0.002	0.112	0.114	-	1V5 (Digital)
		VCCAUX_SMON	1.5	1.455 - 1.545	100%	0.002	0	0.002	-	1V5 (Digital)
		VCC_FUSE	1.8	1.710 - 1.890	-			0.165	-	
Low Power Domain (LPD)										
		VCC_PSLP	0.8	0.775 - 0.825	33%	0.007	0.21	0.217	-	0V80 (Digital)
		VCCO_502	1.8V	1.710 - 1.890	100%	0	0	0	-	1V8_VCCO (Digital)
Full Power Domain (FPD)										
		VCC_PSFP	0.8	0.775 - 0.825	33%	0.014	0.838	0.852	-	0V80 (Digital)
System Power Domain (SPD)										
	Auxiliary	VCCAUX	1.5	1.455 - 1.545	33%	1.115	0.289	1.404	-	1V5 (Digital)
		VCC_SOC	0.8	0.775 - 0.825	33%	0.109	2.457	2.566	-	0V80 (Digital)
	Core	VCC_IO	0.8	0.775 - 0.825	33%	0.016	0.595	0.611	-	0V80 (Digital)
Programmable Logic (PL)										
		VCCINT	0.8	0.775 - 0.825	25%	0.342	41.157	41.499	-	0V80 (Digital)
	Core	VCC_RAM	0.8	0.775 - 0.825	33%	0.02	0.354	0.374	-	0V80 (Digital)
		VCCO 3.3V	3.3	3.135 - 3.400	100%				-	3V3_VCCO (Digital)
		VCCO 2.5V	2.5	2.375 - 2.625	100%				-	2V5_VCCO (Digital)
		VCCO 1.8V	1.8	1.710 - 1.890	100%				-	1V8_VCCO (Digital)
		VCCO 1.5V	1.5	1.425 - 1.575	100%				-	1V5_VCCO (Digital)
		VCCO 1.35V	1.35	1.283 - 1.418	100%				-	1V35_VCCO (Digital)
		VCCO 1.2V	1.2	1.140 - 1.260	100%	0.019	2.03	2.05	-	1V2_VCCO (Digital)
		VCCO 1.1V	1.1	1.045 - 1.155	100%				-	1V1_VCCO (Digital)
	IO	VCCO 1.0V	1	0.950 - 1.050	100%				-	1V0_VCCO (Digital)
		GTY_AVCC	0.88	0.854 - 0.906	70%	0.271	3.071	3.341	-	0V88 (Analog)
		GTY_AVTT	1.2	1.164 - 1.236	70%	0.053	6.027	6.08	-	1V2 (Analog)
	GTY	GTY_AVCCAUX	1.5	1.455 - 1.545	70%	0.001	0.073	0.074	-	1V5 (Analog)

Figure 3.10: Power estimate summary of power rails in XPE tool.

rails are connected to the monitoring channels of ADM1266. The power rail can be shut off, according to the designed strategy, if under-voltage or over-voltage (the threshold can be configured by user) is detected. Current sensors are used on each power rail, and INA226 [17] is used to read out the current and send it to FPGA or SMBUS through I2C bus. Temperature sensor TMP435 [18] is used for remote and local temperature monitoring of the LTM4638, LTM4642 and board temperature. The temperature information can be read out through the I2C bus.

Table 3.8: Power rail currents and power.

				FPGA	FireFly Y12-25 x2	FireFly B04-25	Si5345 x2	DDR4	QSPI x2	DP83867
Power rail	Voltage (V)	Current (A)	Power (W)	Component current (A)						
VCCINT	0.8	44.3	35.44	44.3						
PHY_VDD1PV0	1	0.11	0.11							0.11
SYS12	1.2	4.1	4.92	2.1				2		
SYS15	1.5	1.6	2.4	1.6						
SYS18	1.8	1.37	2.466	0.2		0.7	0.37			0.1
SYS25	2.5	0.49	1.225					0.35		0.14
SYS33	3.3	5.8	19.14		5	0.35	0.25		0.2	
SYS38	3.8	1	3.8		1					
MGTAVCC	0.88	3.4	2.992	3.4						
MGTAVTT	1.2	6.1	7.32	6.1						
MGTYVCCAUX	1.5	0.007	0.0105	0.007						
DDR4_VTT	0.6	1.5	0.9					1.5		
Total power			80.7							

Table 3.9: Power scheme including component efficiencies and power-up sequence.

Module	Rail	Nominal voltage (V)	Power Rail	PMBUS	Board power rails	Current rating (A)	Current consumption (A)	Sequence	Efficiency	Power (W)
LTM4700	1&2	0.8	VCCINT	Y	VCC_INT, VCC_RAM,VCC_SOC, VCC_IO, VCC_PSLP, VCC_PSFP	100	44.3	2	0.85	41.7
LTM4638	1	1.2	MGTAVTT	N	MGTYAVTT,MGTAVTTRCAL	15	6.1	6	0.91	8.0
LTM4638	1	1.2	SYS12	N	SYS_12, VCCO_12	15	4.1	1	0.91	5.4
LTM4638	1	0.88	MGTAVCC	N	MGTY_AVCC	15	3.4	4	0.87	3.4
LTM4638	1	1.8	SYS18	N	SYS_18	15	1.4	1	0.8	3.2
LTM4638	1	1.5	SYS15	N	VCCAUX, VCCAUX_PMC, VCCAUX_SMON	15	1.6	3	0.83	2.9
LTM4638	1	3.3	SYS33	N	SYS_33	15	5.8	NA, SET TO 0	0.91	21.0
LTM4642	1	3.8	SYS38	N	SYS_38	4	1	NA, SET TO 0	0.8	4.8
	2	2.5	SYS25	N	SYS_25	4	0.49	NA, SET TO 0	0.8	1.5
ADP124	1	1.5	MGTY_VCCAUX	N	MGTY_VCCAUX	0.5	0.007	5	0.8	0.0
TPS51200	1	0.6	DDR4_VTT_PL	N	DDR4_VTT_PL	3	1.5	2	0.85	1.1
PCIe conn		3.3	VCC3V3_AUX	N	VCC3V3_AUX		0.05	NA	1	0.2
TPSM5601	1	5	VCC5V	N	VCC5V	1.5	0.5	NA, SET TO 0	0.92	2.7
LT1931IS5	1	-5	VCC5VM	N	VCC5VM	0.27	-0.1	NA, SET TO 0	0.75	0.7
Total power										96.6

3.5.2.1 Power ripple measurements

The FPGA, and in particular its multi-gigabit transceivers, are sensitive to noise in the power rails. According to Xilinx Power Design Manager the ripple on digital I/O power rails (VCCO) such as sys12, sys15, sys18 and sys33 should be less than 4%; on the 0.8 V VCCINT it should not exceed ±17 mV; on analog power rails as MGTAVCC, MGTAVTT and MGTVCCAUX it should be less than 10 mV. In the 3.8 V rail for FireFly modules, the ripple is required to be less 10 mV as well. To verify that all requirements are met, ripples have been measured with an oscilloscope through the SMP connectors available for each rail. The scope was set to DC-coupling, 50 Ω termination and 20 MHz bandwidth. Peak-to-peak ripple measurements for all power rails are shown in Figures 3.11 and 3.12 and are summarized in Table 3.10. Measurements are compliant with requirements.

Table 3.10: Peak-to-peak ripple measurement for all power rails.

Power rail	peak-to-peak (mV)	Power rail	peak-to-peak (mV)
1.2 V	6.5	VCCINT 8.8 V	4.3
1.5 V	7.5	MGTAVCC	6.4
1.8 V	6.9	MGTAVTT	5.7
3.3 V	6.7	MGTVCCAUX	2
3.8 V	8.5	DDR4 0.6 V	2

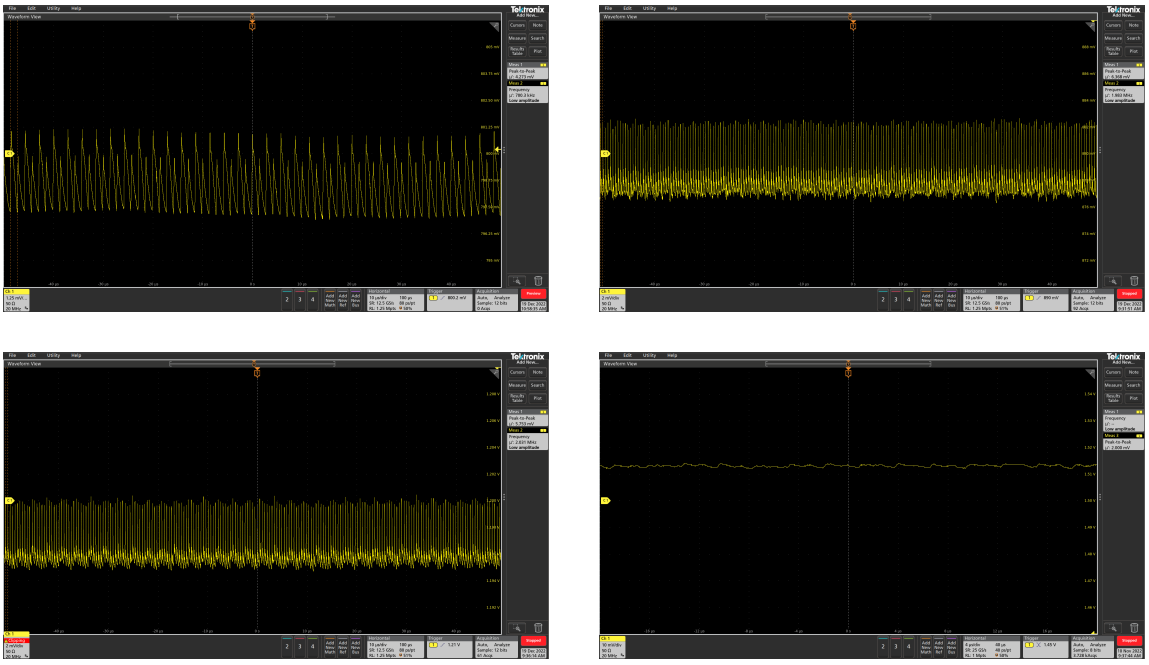


Figure 3.11: Ripple measurement for VCCINT, MGTAVCC, MGTAVTT and MGTVCCAUX power rails.

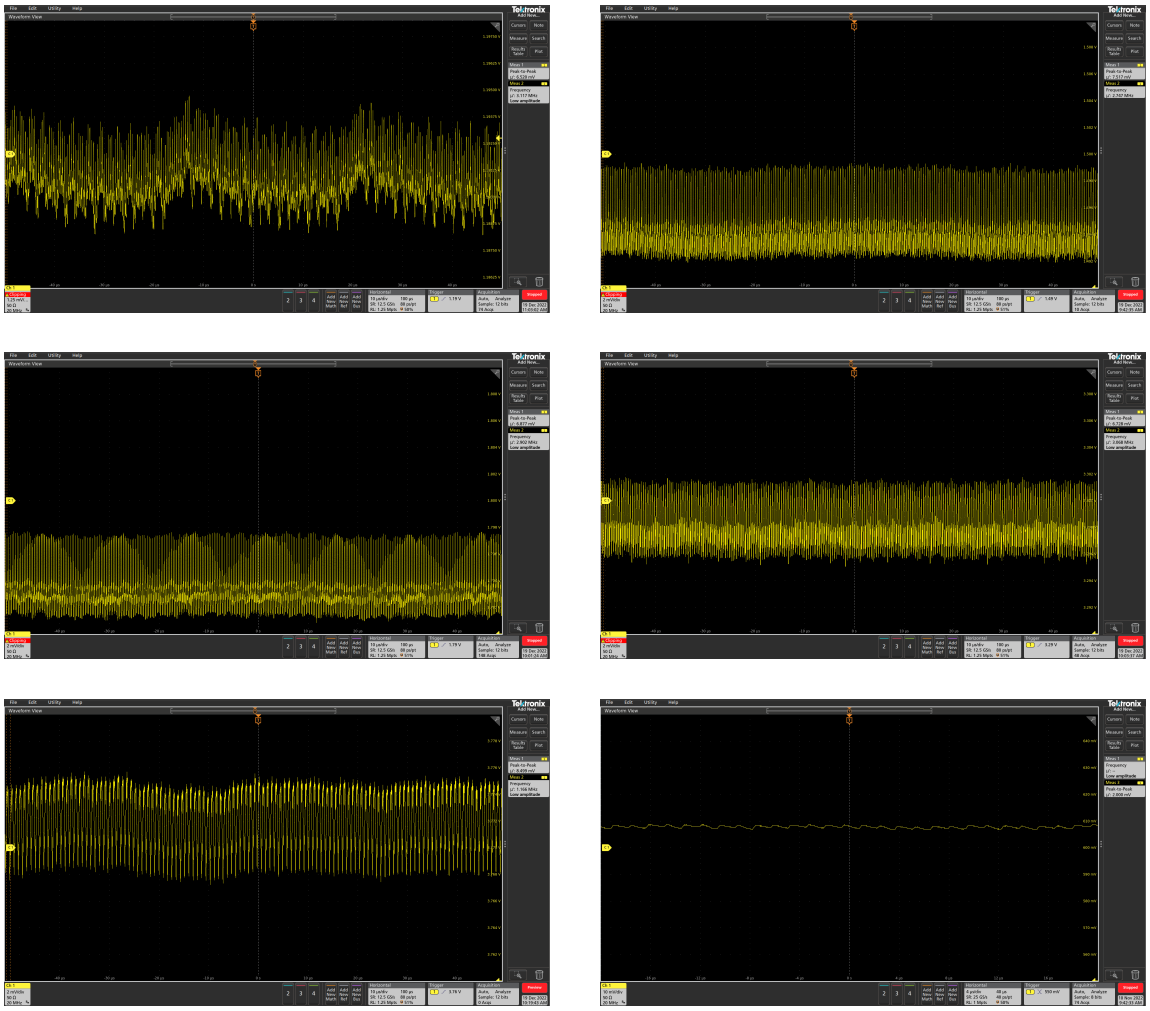


Figure 3.12: Ripple measurement for sys12, sys15, sys18, sys33, Firefly 3.8 V, and DDR4 power rails.

3.6 Thermal Management

3.6.1 Thermal Management for FPGA

Three heatsinks have been designed for FLX-182: two fansinks using fans from different manufacturers and a passive heatsink.

One fansink assembly, S08ESL0R-A, is shown in Figure 3.13. The Cofan F-6010HH12BII-Rev-B fan, shown Figure 3.14, uses a three-wire connector for the 12 V power, ground and the tachometer output. The fan speed is around 4800 rpm. The mean time to failure (MTTF) at 40 ℃ is about 72 years, while after 10 years, 10% of fans are estimated to malfunction[1]. The thermal simulation for this fansink for 70 W of FPGA power consumption is shown in Figure 3.15: the expected FPGA temperature 67 ℃.

The second fansink assembly, S08ESLOR-B, is shown in Figure 3.16. The fan is Sanyo San Ace 9GA0612H9001, it uses the same three-wire connector as the Cofan fan and it is rated for 5000 rpm. Other specifications are listed in the product brief reported in Figure 3.17. The mean time to failure (MTTF) estimated by Sanyo from reported failures is over 100 years. The lifetime, expressed as time until the failure of 10% of fans, is reported to be 8 years at 40 ℃, 4.6 years at 60 ℃. The thermal simulation for this fansink at 70 W power consumption is shown in Figure 3.18: the expected FPGA temperature 70 ℃.

The passive heatsink S08ESL0M of Figure 3.19 can be used if airflow in the chassis of the host server is around 450 LFM. The thermal simulation for a 70 W power consumption is shown in Figure 3.20 and results in an expected FPGA temperature of 54 ℃. Given the various types of host computers used in laboratories, not necessarily able to guarantee sufficient airflow, the fansink has been preferred for prototype samples (Sanyo fan in the last revision).

In all cases, the phase change thermal interface material TPCM585 by Laird Technologies is interposed between heatsink and FPGA and four push-pins are be used to hold the heatsink in place. Temperature measurements for each cooling solution in a production-like environment are presented in Section 3.6.3.

3.6.2 Thermal Management for FireFly Modules

The worst case for ECUO FireFly module is about 2 W for ECUO-Y12-16 and 4.5 W for ECUO-Y12-25. The airflow and temperature simulation for the ECUO-Y12-16 and ECUO-Y12-25 are shown in Figure 3.21. Based on the diagram, the standard pin-fin heatsink will be chosen for ECUO-Y12-16 and high performance pin-fin heatsink will be used for ECUO-Y12-25.

[1] This information has been provided in private communications with the manufacturer and supersedes the mean time between failures (MTBF) reported in the technical drawing.

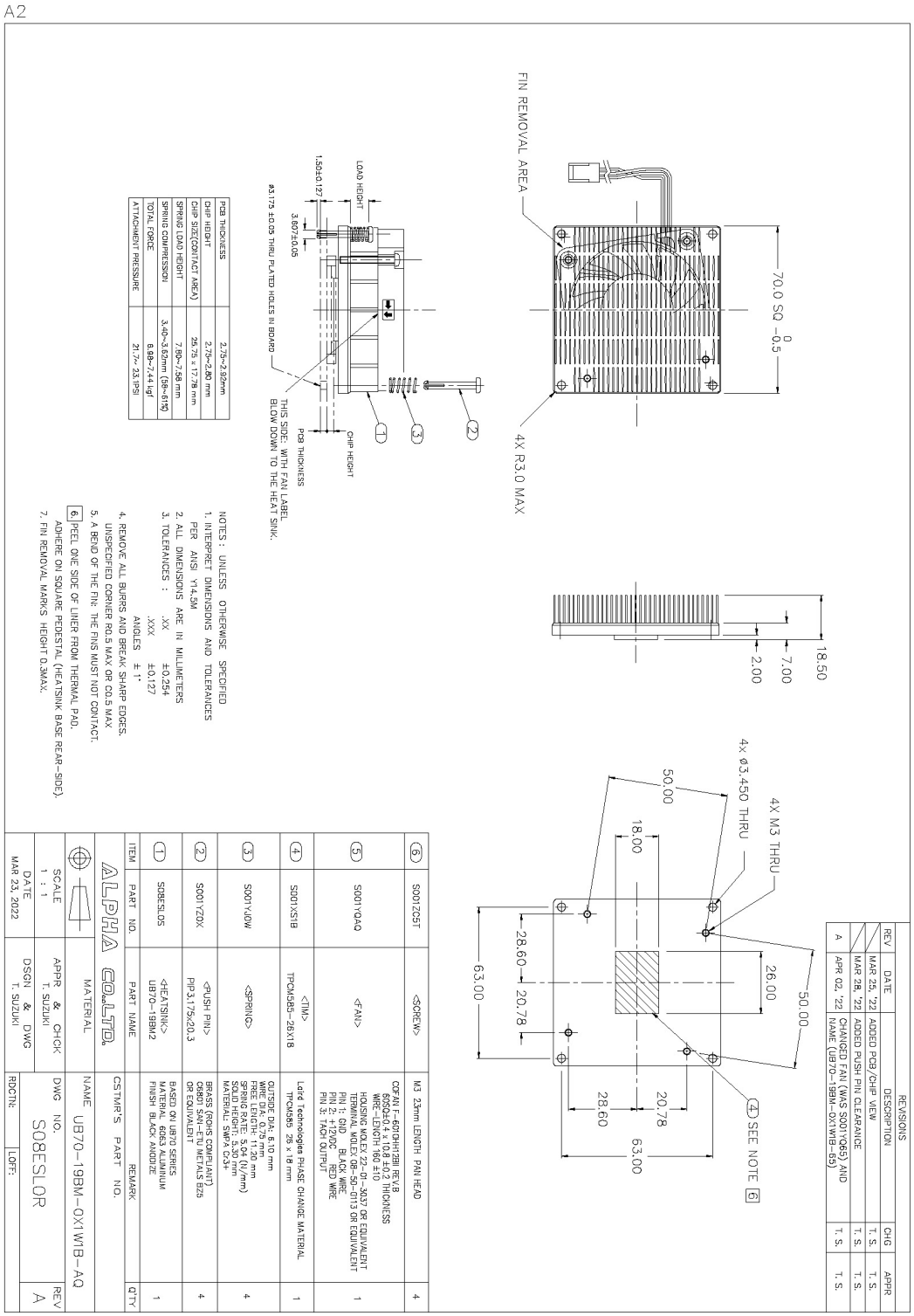


Figure 3.13: FLX-182 FPGA fansink for Cofan fan.

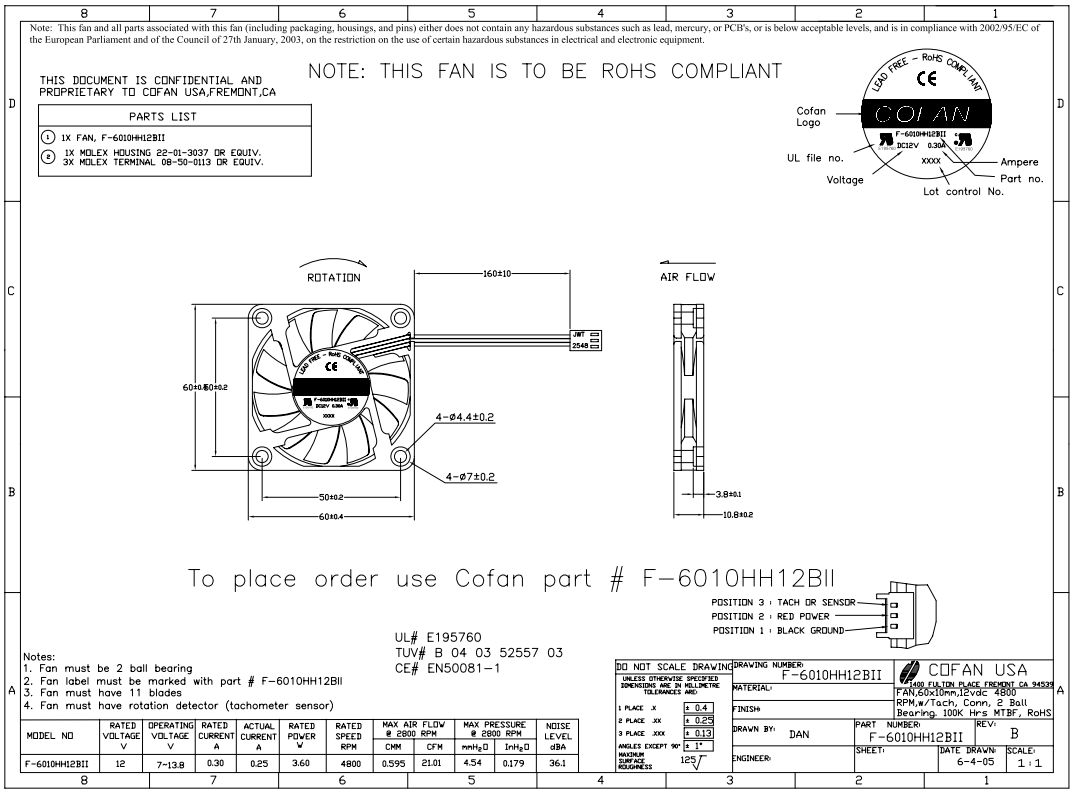


Figure 3.14: FLX-182 FPGA fan by Cofan.

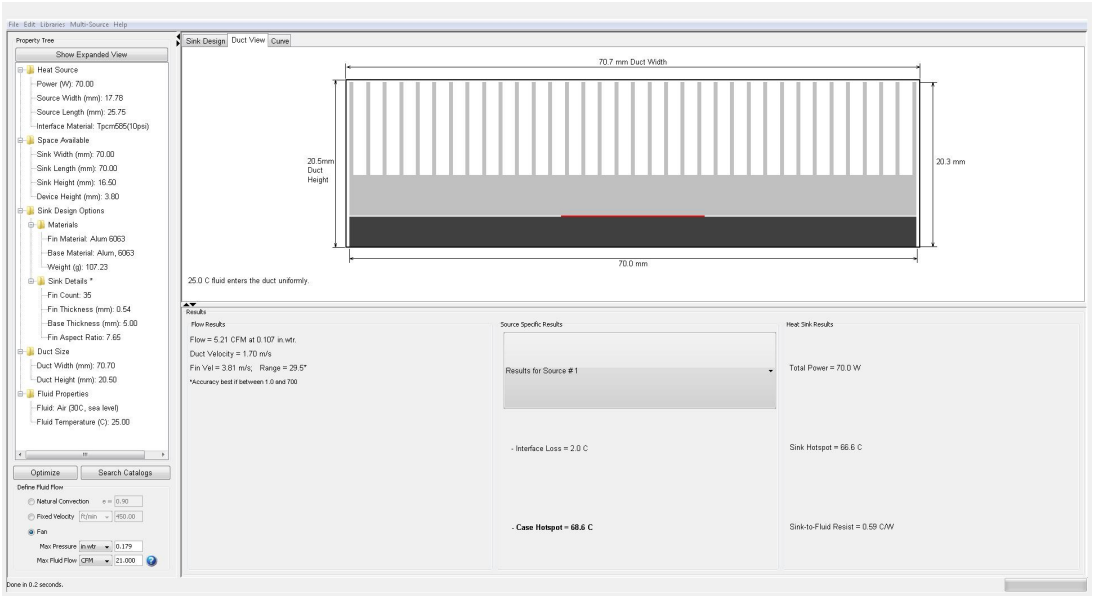


Figure 3.15: FLX-182 FPGA fansink simulation for Cofan fan.

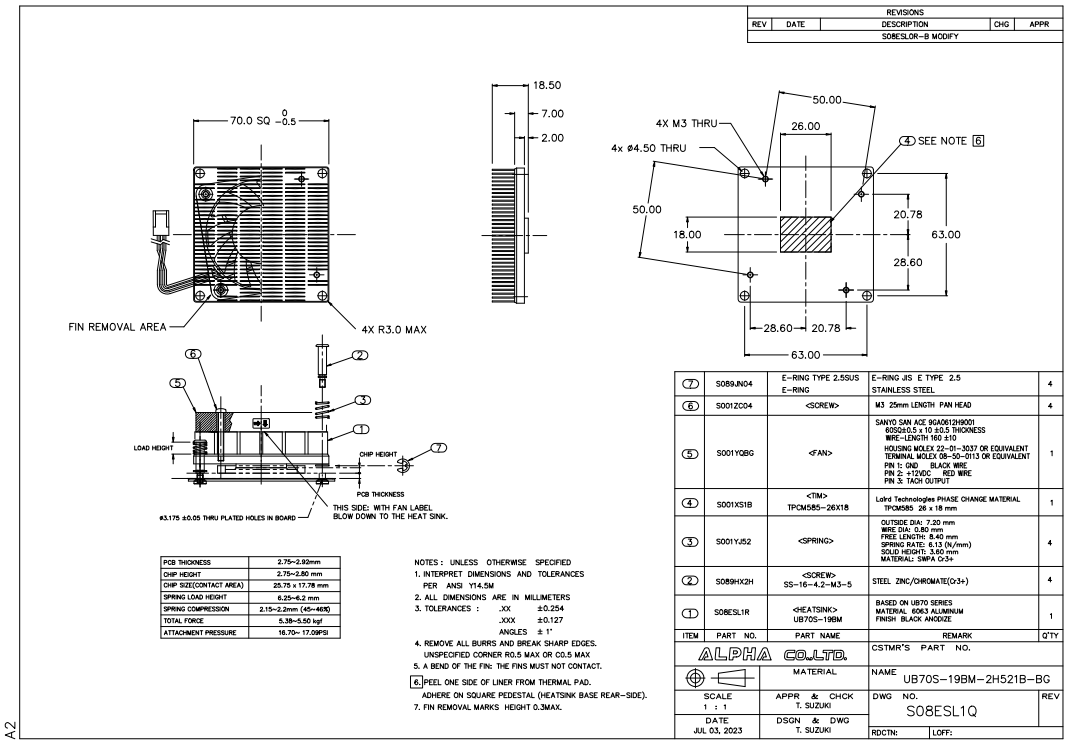


Figure 3.16: FLX-182 FPGA fansink for Sanyo fan.

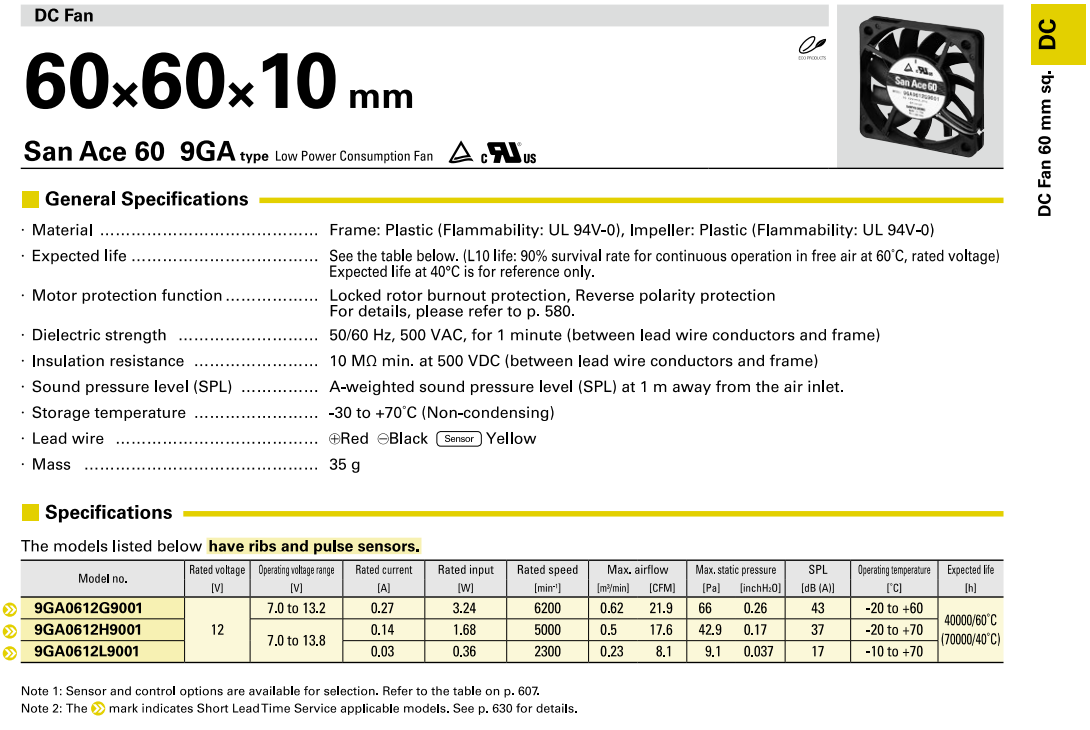


Figure 3.17: Sanyo fan product brief.

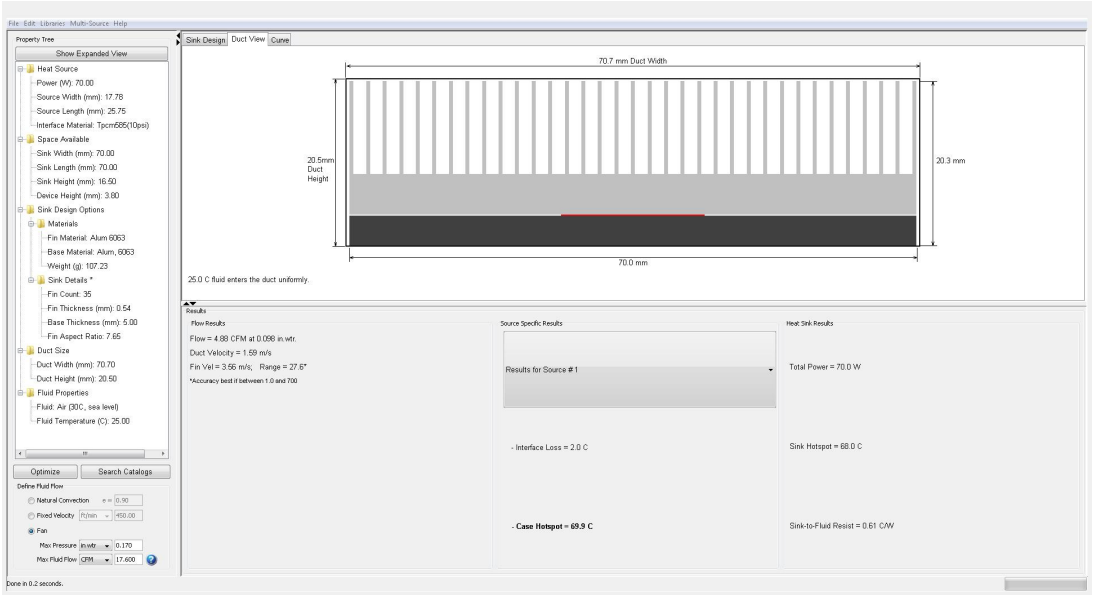


Figure 3.18: FLX-182 FPGA fansink simulation for Sanyo fan.

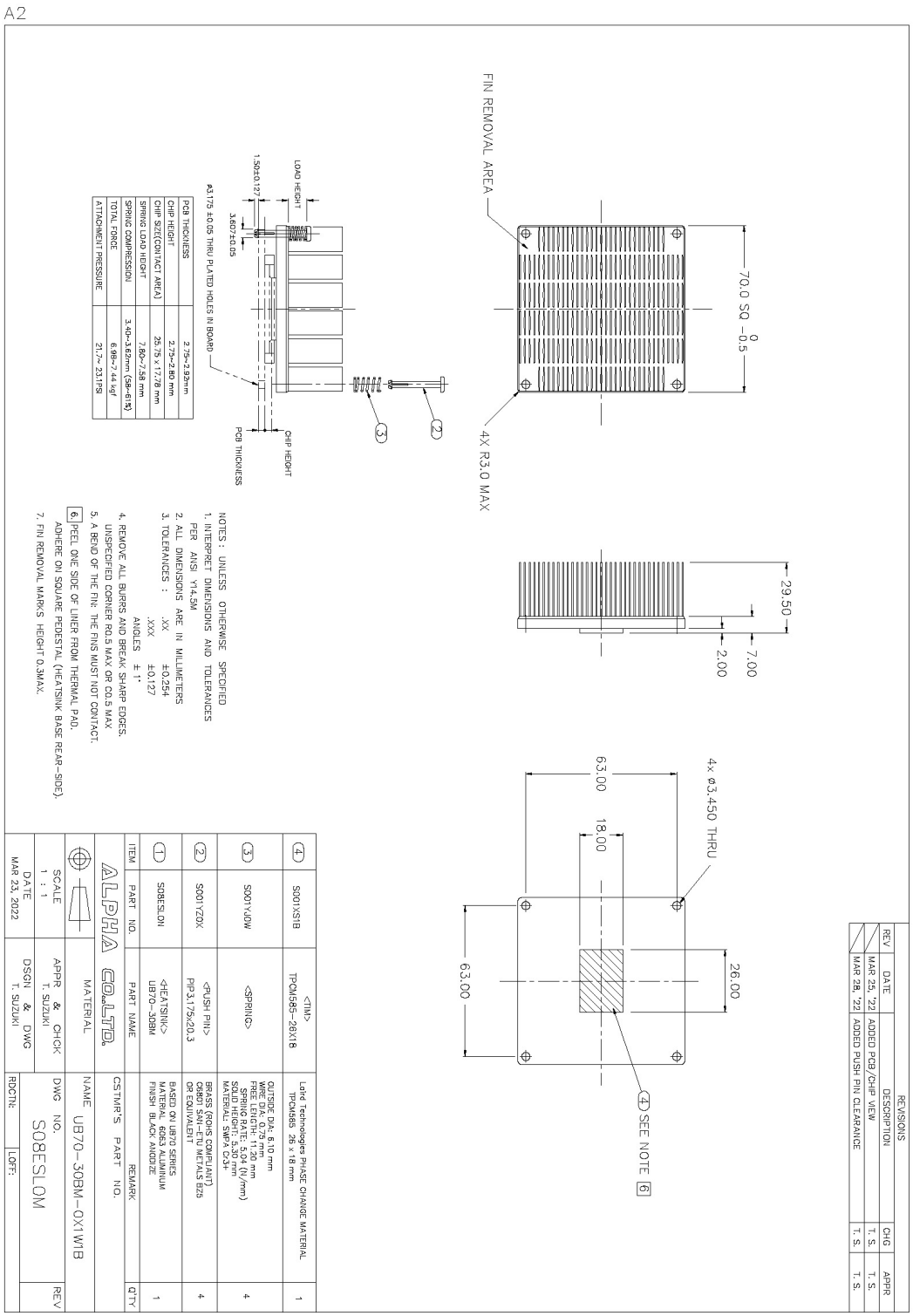


Figure 3.19: FLX-182 FPGA passive heatsink technical drawing.

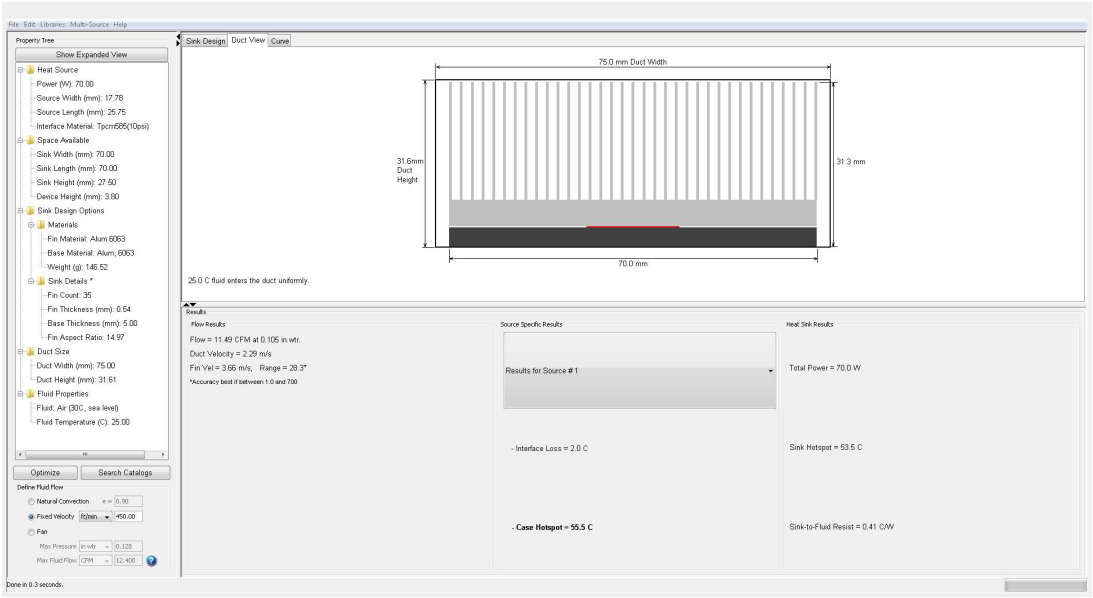
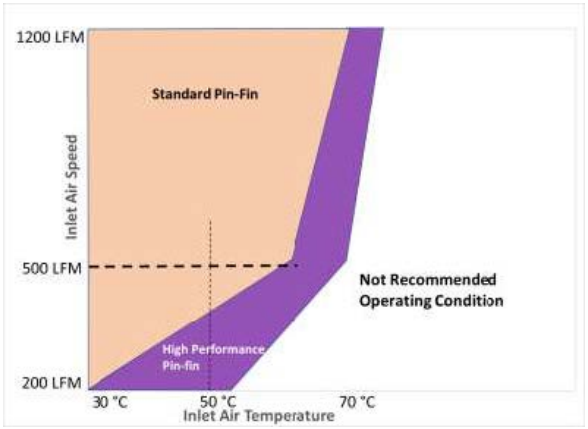


Figure 3.20: FLX-182 FPGA passive heatsink simulation.



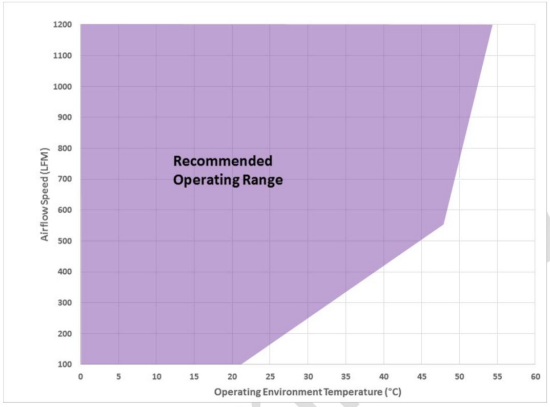


Figure 11. Required Airflow vs. Inlet Air Temperature

Figure 3.21: Temperature vs airflow diagram for (a) FireFly ECUO-Y12-16, (b) ECUO-Y12-25.

3.6.3 TEMPERATURE MEASUREMENTS

FPGA and FireFly module temperatures have been measured in an environment similar to production. The goal was to test whether the FPGA temperature remained below 70 ℃ and the FireFly modules below 50 ℃ with each of the heatsinks presented above. FLX-182 number 0005, with ECUO-Y12-16, has been installed in a 2U Supermicro H12 server in the CERN TDAQ Testbed. The server is located in a 19-inch rack with horizontal cooling. The FLX-182 was installed above a 200 Gb/s network interface as shown in Figure 3.25 and programmed with FULLMODE firmware. During each temperature measurement session FLX-182 received data (64 B messages at 1 MHz) on all 24 links from an FLX-712 programmed as emulator. Data was read out by software in the host server. The server fan were set to full speed as customary for ATLAS operations. The temperature of the laboratory was stable at 19 ℃ during all measurements. Each measurement session lasted for at least 30 minutes after temperatures stabilized. FireFly modules temperatures were obtained with software tools running on the host, the FPGA temperature by reading the appropriate special file in PetaLinux.

The time-averaged temperatures are reported in Table 3.11. The relatively high temperature of the ECUO-B04-28 TXRX module is due to the use of a regular pin-fin heatsink instead of the taller high-performance one. The FPGA and FireFly temperatures are comparable with all cooling solutions.

The main advantage of a fansink is the redundancy in case of server fan failures. However to have a sizeable temperature increase two of the three server fans had to be removed. In that case the FPGA temperature did not exceed 60 ℃ with either the Sanyo fansink or the passive heatsink (Figure 3.22). The FireFly modules instead approached 70 ℃, a temperature within working range but harmful in terms of component lifetime. Given the extremely low likelihood of a simultaneous failure of two server fans, the passive heatsink is to be considered as an option for the production FELIX I/O card.

Table 3.11: FPGA and FireFly modules temperature in a production-like configuration..

	Component temperature (℃)					
	FPGA (±1)	FFLY TX1 (±3)	FFLY TX2 (±3)	FFLY RX1 (±3)	FFLY RX2 (±3)	FFLY TXRX (±3)
Cofan fan	42	38	39	44	43	48
Sanyo fan	42	37	41	44	43	49
Passive	45	35	36	42	40	46

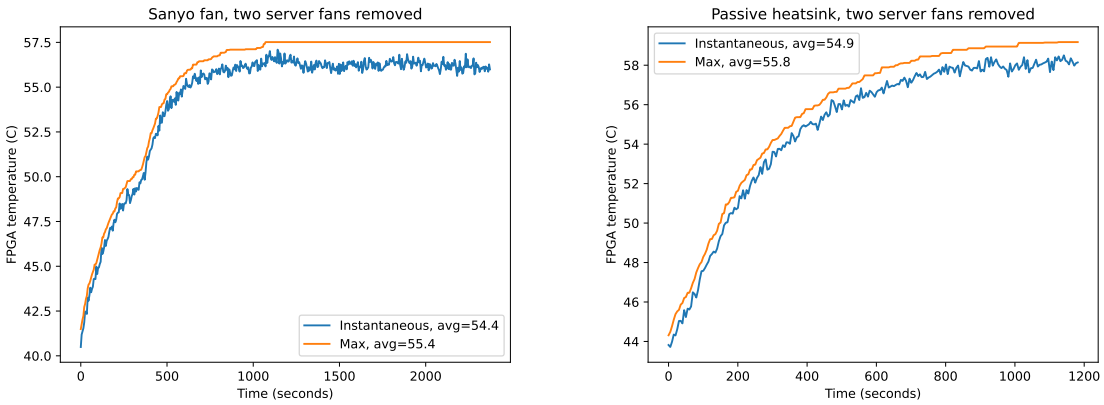


Figure 3.22: FPGA temperature with Sanyo fansink (a) and passive heatsink (b) with two server fans removed.

3.7 MECHANICAL DESCRIPTION

FLX-182 is a full-height, full-length PCI Express card of height 111 mm and length 312 mm. The thickness is 2.92 mm. Since the PCIe slot can only support the board with thickness of 1.57 mm, the PCB top layers are milled down to layers 1 to 10 in the gold finger area. The board size is shown in Figure 3.23.

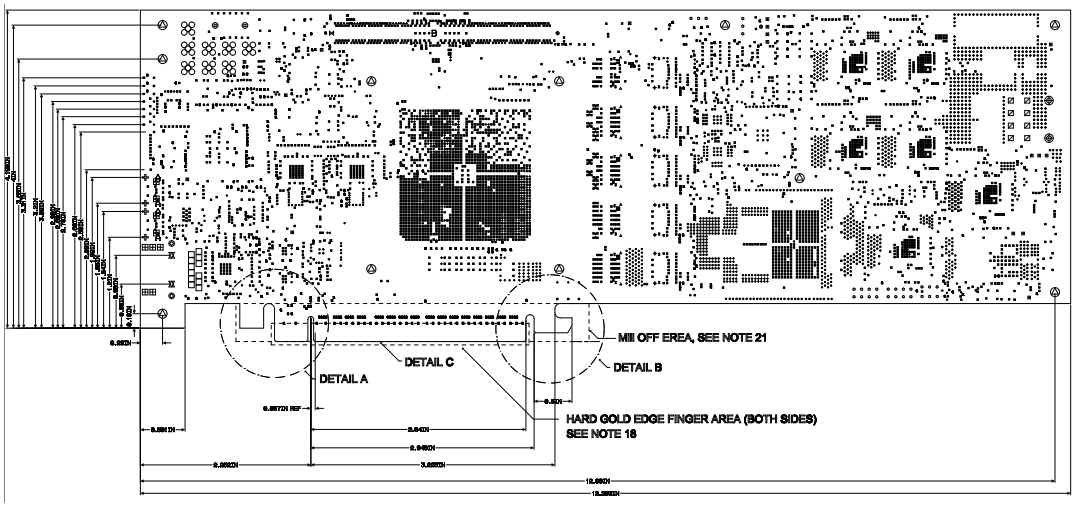


Figure 3.23: Board dimensions.

The FLX-182 front panel is shown in Figure 3.24. It hosts a a pair of MTP-24 connectors, one MTP-12 connector dedicated to the LTI interface, one RJ45 socket, two USB-C sockets for JTAG and UART respectively, and six MMCX connectors. In addition, the front panel exposes the SD card slot and six LEDs. The placement of the removable MMCX connectors is under review to prevent clashes with the host server chassis. Newly produced front panels are planned to be perforated to improve the exhaust airflow. Pictures of a FLX-182 installed on a Supermicro 2U H12 server in the CERN TDAQ Testbed are shown in Figure 3.25.

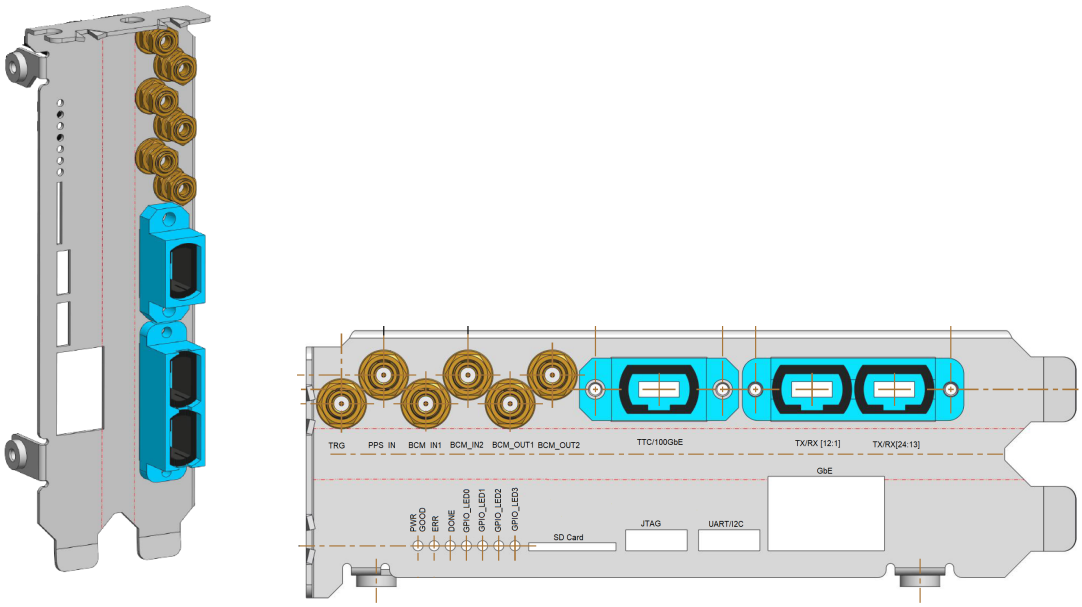


Figure 3.24: Technical drawings of the FLX-182 front panel.

Figure 3.25: FLX-182 (revision 1.0) installed in a Supermicro H12 server, above a 200 GbE Nvidia Connect-X6 network card.

3.8 MANUFACTURER

The PCB vendor for the FLX-182 is SCC Technologies, the assembly is undertaken by AA-Tech. The bill of materials for the FLX-182 is listed in Table 3.12. These tables list part numbers, manufacturers, and quantities needed for a single board.

Table 3.12: Bill of materials for FLX-182.

QTY	Manufacturer	Part Number	Distributor	Description
2	Molex	22-11-1031	Digi-Key	CONN HEADER VERT 3POS 2.5MM
1	Molex	878321420	Digi-Key	CONN HEADER SMD 14POS 2MM
1	Littelfuse Inc.	0448012.MR	Digi-Key	FUSE BRD MNT 12A 85VAC/VDC 2SMD
1	MOLEX	503398-1892	Digi-Key	MicroSD SMT Push-Push 1.28mm height MicroSD SMT Push-Push 1.28mm height
1	ECS	ECS-LVDS25-2000-A		XTAL OSC XO 200.0000MHZ LVDS SMD
7	MOLEX	734151472	Digi-Key	RF Connectors / Coaxial Connectors MMCX Vrt Jack PCB 50Ohms
2	TXC CORPORATION	7M48072002	Digi-Key	CRYSTAL 48.0000MHZ 8PF SMD
1	Microchip Technology	93LC56B-I/SN	Digi-Key	IC EEPROM 2K SPI 2MHZ 8SOIC
2	Analog Devices	AD5662BRMZ-1	Digi-Key	AD5662BRMZ-1, 16 bit-Bit DAC 1.2Msps, SPI, Microwire, 8-Pin MSOP
1	Analog Devices	ADCMP561BRQZ	Digi-Key	ADCMP561BRQZ, Dual Comparator Complementary 16-Pin QSOP
1	Analog Devices	ADM1266ACPZ	Digi-Key	IC SUPERVISOR 12 CHANNEL 48TQFP
2	Analog Devices	ADP125ARHZ	Digi-Key	IC REG LIN POS ADJ 500MA 8MSOP
1	Analog Devices	ADR4533ARZ	Digi-Key	Analog Devices ADR4533ARZ, Series Voltage Reference 3.3V, +/-0.04% 15 V max., 8-Pin SOIC
1	Samsung Electro-Mechanics	CL03A104KP3NNNC	Digi-Key	CAP CER 0.1UF 10V X5R 0201
4	AVX Corporation	0201ZD105MAT2A	Mouser	CAP CER 1UF 10V X5R 0201
8	TDK Corporation	C1005X7R1E102K050BA	Digi-Key	CAP CER 1000PF 25V X7R 0402
76	TDK Corporation	C1005X8R1E103K050BA	Mouser	CAP CER 10000PF 25V X8R 0402
1	KEMET	C0402C223K5RACTU	Digi-Key	CAP CER 0.022UF 50V X7R 0402
221	Samsung Electro-Mechanics	CL05B104KA5NNNC	Digi-Key	CAP CER 0.1UF 25V X7R 0402
32	Taiyo Yuden	JMK105B7224KV-F	Digi-Key	CAP CER 0.22UF 6.3V X7R 0402

Table 3.12 continued from previous page

QTY	Manufacturer	Part Number	Distributor	Description
1	Taiyo Yuden	JMK105B7474KVHF	Digi-Key	CAP CER 0.47UF 6.3V 10% X7R 0402
1	TDK Corporation	CGA2B2C0G1H100D050BA		CAP CER 10PF 50V C0G 0402
68	Murata Electronics	GRJ155R60J106ME11D	Digi-Key	CAP CER 10UF 6.3V X5R 0402
6	Yageo	CC0402KRX7R9BB151	Digi-Key	CAP CER 150PF 50V X7R 0402
2	Kemet	C0402C180K5RAC7867	Digi-Key	CAP CER 18PF 50V X7R 0402
83	TDK Corporation	C1005X5R1E105K050BC	Digi-Key	CAP CER 1UF 25V X5R 0402
6	TDK Corporation	C1005X5R1E105K050BC	Digi-Key	CAP CER 1UF 25V X5R 0402
1	Yageo	CC0402KRX7R8BB222	Digi-Key	CAP CER 2200PF 25V X7R 0402
7	Taiyo Yuden	LMK105BJ225MV-F	Digi-Key	CAP CER 2.2UF 10V X5R 0402
2	Kemet	C0402C220K5GACTU	Digi-Key	CAP CER 22PF 50V C0G/NP0 0402
2	Kemet	C0402C270K5GACTU	Digi-Key	CAP CER 27PF 50V C0G/NP0 0402
17	Murata Electronics	GRM155R61A475MEAAD	Digi-Key	CAP CER 4.7UF 10V X5R 0402
2	AVX Corporation	04023A680JAT2A	Digi-Key	CAP CER 68PF 25V NP0 0402
2	Samsung Electro-Mechanics	CL10A106KP8NNNC	Digi-Key	CAP CER 10UF 10V X5R 0603
6	Samsung Electro-Mechanics	CL10A226MQ8NRNC	Digi-Key	CAP CER 22UF 6.3V X5R 0603
48	Murata Electronics	GRM188R60J476ME15D	Digi-Key	CAP CER 47UF 6.3V X5R 0603
35	Murata Electronics	GRM21BR60J107ME15L	Digi-Key	CAP CER 100UF 6.3V X5R 0805
6	TDK Corporation	CGA4J3X7R1E105M125AB	Digi-Key	CAP CER 1UF 25V X7R 0805
6	Samsung Electro-Mechanics	CL21A225KAFNNNG	Digi-Key	CAP CER 2.2UF 25V X5R 0805
69	Murata Electronics	GRM21BR61E226ME44K	Digi-Key	CAP CER 22UF 25V X5R 0805
2	KEMET	C0805C472J3GEC7210	Digi-Key	CAP CER 0805 4.7NF 25V C0G 5%
2	Samsung Electro-Mechanics	CL21A475KAQNNNE	Digi-Key	CAP CER 4.7UF 25V X5R 0805
6	Taiyo Yuden	JMK212BBJ476MG-T	Digi-Key	CAP CER 47UF 6.3V X5R 0805
4	Murata Electronics	GRM21BR61A476ME15L	Digi-Key	CAP CER 47UF 10V X5R 0805
16	Taiyo Yuden	JMK316ABJ107ML-T	Digi-Key	CAP CER 100UF 6.3V X5R 1206
18	Murata Electronics	GRM31CR60E227ME11L	Digi-Key	CAP CER 220UF 2.5V X5R 1206
8	Murata Electronics	GRT31CR61E226ME01L	Digi-Key	CAP CER 22UF 25V X5R 1206

Table 3.12 continued from previous page

QTY	Manufacturer	Part Number	Distributor	Description
1	TDK Corporation	C3216X5R1E476M160AC	Digi-Key	CAP CER 47UF 25V X5R 1206
8	Murata Electronics	GRM32ER60G337ME05L	Digi-Key	CAP CER 330UF 4V X5R 1210
5	Vishay Sprague	597D227X0025M2T		CAP TANT 220UF 20% 25V 3226
9	KEMET	T495X107K025ATE150		CAP TANT 100UF 10% 25V 2917
20	Vishay Sprague	TMCME0J477MTRF	Digi-Key	CAP TANT 470UF 20% 6.3V 2917
318	Yageo	RC0402FR-070RL	Digi-Key	RES SMD 0 OHM JUMPER 1/16W 0402
1	Stackpole Electronics Inc	CSS0402FT2L50	Digi-Key	RES SHUNT, 0402, 0.0025 OHM, 1%,
1	YAGEO	RC0402FR-071K2L	Digi-Key	RES 1.2K OHM 1% 1/16W 0402
28	Panasonic	ERJ-2RKF1000X	Digi-Key	RES SMD 100 OHM 1% 1/10W 0402
3	Panasonic	ERJ-2RKF1000X	Digi-Key	RES SMD 100 OHM 1% 1/10W 0402
12	Yageo	RC0402FR-07100KL	Digi-Key	RES SMD 100K OHM 1% 1/16W 0402
7	Yageo	RC0402FR-07100KL	Digi-Key	RES SMD 100K OHM 1% 1/16W 0402
43	Yageo	RC0402FR-0710KL	Digi-Key	RES SMD 10K OHM 1% 1/16W 0402
49	Yageo	RC0402FR-0710KL	Digi-Key	RES SMD 10K OHM 1% 1/16W 0402
1	Yageo	RC0402FR-0711K3L	Digi-Key	RES 11.3K OHM 1% 1/16W 0402
1	Yageo	RC0402FR-07113KL	Digi-Key	RES SMD 113K OHM 1% 1/16W 0402
5	Yageo	RC0402FR-0711KL	Digi-Key	RES SMD 11K OHM 1% 1/16W 0402
2	Yageo	RC0402FR-07127RL	Digi-Key	RES 127 OHM 1% 1/16W 0402
1	Yageo	RC0402FR-0712KL	Digi-Key	RES SMD 12K OHM 1% 1/16W 0402
1	Yageo	RC0402FR-0719K1L	Digi-Key	RES SMD 19.1K OHM 1% 1/16W 0402
46	Yageo	RC0402FR-071KL	Digi-Key	RES SMD 1K OHM 1% 1/16W 0402
17	Yageo	RC0402FR-071KL	Digi-Key	RES SMD 1K OHM 1% 1/16W 0402
1	Yageo	RC0402FR-071ML	Digi-Key	RES SMD 1M OHM 1% 1/16W 0402
1	YAGEO	RC0402FR-072R2L	Digi-Key	RES 2.2 OHM 1% 1/16W 0402
2	Yageo	RC0402FR-072K21L	Digi-Key	RES SMD 2.21K OHM 1% 1/16W 0402
7	Yageo	RC0402FR-072K49L	Digi-Key	RES SMD 2.49K OHM 1% 1/16W 0402

Table 3.12 continued from previous page

QTY	Manufacturer	Part Number	Distributor	Description
3	Yageo	RC0402FR-0722K6L	Digi-Key	RES SMD 22.6K OHM 1% 1/16W 0402
18	Yageo	RC0402FR-07240RL	Digi-Key	RES SMD 240 OHM 1% 1/16W 0402
2	Yageo	RC0402FR-07261RL	Digi-Key	RES SMD 261 OHM 1% 1/16W 0402
4	Yageo	RC0402FR-072KL	Digi-Key	RES SMD 2K OHM 1% 1/16W 0402
1	Yageo	RC0402FR-073K48L	Digi-Key	RES SMD 3.48K OHM 1% 1/16W 0402
6	Yageo	AC0402FR-0730RL	Digi-Key	RES SMD 30 OHM 1% 1/16W 0402
1	Yageo	RC0402FR-0732K4L	Digi-Key	RES SMD 32.4K OHM 1% 1/16W 0402
6	Yageo	RC0402FR-07330RL	Digi-Key	RES SMD 330 OHM 1% 1/16W 0402
1	Yageo	RC0402JR-073KL	Digi-Key	RES 3K OHM 5% 1/16W 0402
1	Yageo	AC0402FR-074M7L	Mouser	RES 4.7M OHM 1% 1/16W 0402
110	Yageo	RC0402FR-074K7L	Digi-Key	RES SMD 4.7K OHM 1% 1/16W 0402
17	Yageo	RC0402FR-074K7L	Digi-Key	RES SMD 4.7K OHM 1% 1/16W 0402
1	Yageo	RC0402FR-074K99L	Digi-Key	RES SMD 4.99K OHM 1% 1/16W 0402
1	Yageo	RC0402FR-07422KL	Digi-Key	RES 422K OHM 1% 1/16W 0402
1	Yageo	RC0402FR-0747KL	Digi-Key	RES SMD 47K OHM 1% 1/16W 0402
34	Yageo	RC0402FR-0749R9L	Digi-Key	RES 49.9 OHM 1% 1/16W 0402
1	Yageo	RC0402FR-0749K9L	Digi-Key	RES SMD 49.9K OHM 1% 1/16W 0402
1	Yageo	RC0402FR-07499RL	Digi-Key	RES SMD 499 OHM 1% 1/16W 0402
4	Yageo	RC0402FR-075K11L	Digi-Key	RES 5.11K OHM 1% 1/16W 0402
1	Yageo	RC0402FR-075K76L	Digi-Key	RES SMD 5.76K OHM 1% 1/16W 0402
1	Yageo	RC0402FR-0751RL	Digi-Key	RES 51 OHM 1% 1/16W 0402
38	Yageo	RC0402FR-076K81L	Digi-Key	RES SMD 6.81K OHM 1% 1/16W 0402
4	Yageo	RC0402FR-0769K8L	Digi-Key	RES SMD 69.8K OHM 1% 1/16W 0402
2	Yageo	RC0402FR-0782R5L	Digi-Key	RES 82.5 OHM 1% 1/16W 0402
1	panasonic	ERA-2ARB8250X	Digi-Key	RES SMD 825 OHM 0.1% 1/16W 0402
1	Yageo	RC0402FR-079K09L	Digi-Key	RES 9.09K OHM 1% 1/16W 0402
4	Yageo	RC0603JR-070RL	Digi-Key	RES SMD 0 OHM JUMPER 1/10W 0603

Table 3.12 continued from previous page

QTY	Manufacturer	Part Number	Distributor	Description
2	Yageo	RC0603JR-070RL	Digi-Key	RES SMD 0 OHM JUMPER 1/10W 0603
3	Yageo	RC0603FR-0715RL	Digi-Key	RES SMD 15 OHM 1% 1/10W 0603
1	Yageo	RC0603FR-074K7L	Digi-Key	RES SMD 4.7K OHM 1% 1/10W 0603
1	Yageo	RC0603FR-0740R2L	Digi-Key	RES SMD 40.2 OHM 1% 1/10W 0603
12	Vishay Dale	WSL080500000ZEA9	Digi-Key	RES 0 OHM JUMPER 0805
1	RN732ATTD1293B50	KOA	Mouser	SMD 0805 129 Kohms 0.1%
1	Yageo	RT0805BRD0713K3L	Digi-Key	RES SMD 13.3K OHM 0.1% 1/8W 0805
1	Panasonic	ERJ-PB6B3012V	Digi-Key	RES SMD 30.1K OHM 0.1% 1/4W 0805
1	Yageo	RT0805BRD0740K2L	Digi-Key	RES SMD 40.2K OHM 0.1% 1/8W 0805
2	Panasonic	ERA-6AEB6042V	Digi-Key	RES 60.4K OHM 0.1% 1/8W 0805
5	Vishay Dale	CRCW12060000Z0EBC	Digi-Key	RES 0 OHM JUMPER 1/4W 1206
7	Stackpole Electronics Inc	HCS1206FT1L00	Digi-Key	RES 0.001 OHM 1% 2W 1206
2	Stackpole Electronics Inc	HCS1206FT1L00	Digi-Key	RES 0.001 OHM 1% 2W 1206
3	Stackpole Electronics Inc	HCS1206FT1L00	Digi-Key	RES 0.001 OHM 1% 2W 1206
3	Stackpole Electronics Inc	HCS1206FT1L00	Digi-Key	RES 0.001 OHM 1% 2W 1206
1	Stackpole Electronics Inc	CSNL2010FT1L00	Digi-Key	RES 0.001 OHM 1% 1.5W 2010
1	Stackpole Electronics Inc	CSS2725FTL250	Digi-Key	RES 250 UOHM 1% 4W 2725
1	Silicon Labs	569BAAA000118BBGR	Digi-Key	XTAL OSC VCXO 156.2500MHZ LVDS
1	Silicon Labs	569BAAA000118BBGR	Digi-Key	XTAL OSC VCXO 156.2500MHZ LVDS
1	Molex	1511050001	Digi-Key	CONN SKT MINIDIMM 288POS SMD
1	Diodes Incorporated	DDZ9678-7	Digi-Key	DIODE ZENER 1.8V 500MW SOD123
12	Murata Electronics	DFE252012P-1R0M=P2	Digi-Key	FIXED IND 1UH 4.3A 42 MOHM SMD
1	Texas Instruments	DP83867ISRGZT	Digi-Key	IC CONTROLLER ETHERNET 48VQFN
1	EPSON	FA-238V 12.0000MA-C5	Digi-Key	CRYSTAL 12.0000MHZ 18PF SMD
1	ON Semiconductor	FDN336P	Digi-Key	MOSFET P-CH 20V 1.3A SSOT3
2	Samtec Inc.	UEC5-019-2-H-D-RA-1	Digi-Key	CONN MICRO FLYOVER RCPT 38POS R/A
2	Samtec Inc.	UEC5-019-2-H-D-RA-1	Digi-Key	CONN MICRO FLYOVER RCPT 38POS R/A

Table 3.12 continued from previous page

QTY	Manufacturer	Part Number	Distributor	Description
1	Samtec Inc.	UEC5-019-2-H-D-RA-1	Digi-Key	CONN MICRO FLYOVER RCPT 38POS R/A
5	Samtec Inc.	UCC8-010-1-H-S-1-A	Digi-Key	CONN MICRO FLYOVER RCPT 10P SMD
1	FTDI	FT4232HL-REEL	Digi-Key	IC USB HS QUAD UART/SYNC 64-LQFP
6	Sullins Connector Solutions	PRPC040SAAN-RC	Digi-Key	CONN MICRO FLYOVER RCPT 10P SMD
2	Sullins Connector Solutions	PRPC040SAAN-RC	Digi-Key	CONN HEADER VERT 40POS 2.54MM
2	Laird-Signal Integrity Products	HZ0805E601R-10	Digi-Key	FERRITE BEAD 600 OHM 0805 1LN
10	Texas Instruments	INA226AIDGSR	Digi-Key	IC MONITOR PWR/CURR BIDIR 10MSOP
1	BNL	BNLSD3P0ADPT	BNL	IP4856 SD 3.0 LVL TRANS ADAPT
1	Pulse Electronics Network	J0G-0001NL	Digi-Key	Ethernet Connector 1x1 LOW PROFILE , GIGABIT
1	Digilent, Inc.	410-308-B	Digi-Key	MOD PROGRAMMING JTAG-SMT2-NC
1	Texas Instruments	LMR70503TM_NOPB	TI	SIMPLE SWITCHER 2.8V to 5.5V, 300mA Buck/Boost
6	Analog Devices Inc.	LTM4638IY#PBF	TI	505-LTM4638IY#PBF-ND
1	Analog Devices Inc.	LTM4642EY#PBF	Digi-Key	DC DC CNVRTR 0.6-5.5V 0.6-5.5V
1	Analog Devices Inc.	LTM4700IY	Digi-Key	DUAL 50A SINGLE 100A M REG
22	Lite-On Inc.	LTST-C191KGKT	Digi-Key	LED GREEN CLEAR SMD
1	Lite-On Inc.	LTST-C191KRKT	Digi-Key	LED RED CLEAR SMD
1	Maxim Integrated	MAX6643LBBAEE+T	Digi-Key	IC CNTRLR FAN SPEED 16-QSOP
1	EPSON	FC-13A 32.7680KA-A3	Mouser	CRYSTAL 32.7680KHZ 12.5PF SMD
2	TDK Corporation	MPZ1608S221ATA00	Digi-Key	FERRITE BEAD 220 OHM 0603 1LN
11	TDK Corporation	MPZ1608S221ATA00	Digi-Key	FERRITE BEAD 220 OHM 0603 1LN
2	Micron	MT25QU02GCBB8E12-0SIT TR	Mouser	IC FLASH 2G SPI 133MHZ 24TPBGA
23	ON Semiconductor	NDS331N	Digi-Key	MOSFET N-CH 20V 1.3A SSOT3
2	ON Semiconductor	NLSV4T244MUTAG	Digi-Key	LEVEL TRANSLATOR, 4BIT, UQFN-12
1	Molex	39301080	Digi-Key	CONN HEADER 8POS 4.2MM R/A TIN
1	Nexperia	PMEG3005ELD,315	Mouser	Schottky Diodes & Rectifiers Schottky Diode
2	C&K	SDA04H1SBD	Digi-Key	SWITCH SLIDE DIP SPST 25MA 24V
1	Vishay Siliconix		Digi-Key	MOSFET N-CH 30V 3.6A SOT-23

Table 3.12 continued from previous page

QTY	Manufacturer	Part Number	Distributor	Description
1	Silicon Labs	SI53156-A01AGM	Digi-Key	IC PCIE BUFFER 100MHZ 32QFN
2	Silicon Labs	SI5345A-B-GM	Digi-Key	IC CLK BUFFER PLL 64QFN
1	Silicon Labs	570BBC000121DG	Digi-Key	XTAL OSC XO 100.0000MHZ LVDS SMD
1	Silicon Labs	570BAB000299DG	Digi-Key	XTAL OSC XO 200.0000MHZ LVDS SMD
1	Silicon Labs	570BAB001495DGR	Silicon Labs	XTAL OSC XO 240.474MHZ LVDS SMD
1	Silicon Labs	570JAC000900DGR	Digi-Key	XTAL OSC XO 33.3333333MHZ CMOS
1	Silicon Labs		Silicon Labs	XTAL OSC XO 322.265625MHZ LVDS SMD
2	Silicon Labs	570BAA001495DG	Silicon Labs	XTAL OSC XO 40.0780MHZ LVDS SMD
19	Cinch Connectivity	128-0711-201	Digi-Key	CONN UMC JACK STR 50 OHM SMD
1	Texas Instruments	SN65LVDS100D	TI	2-Gbps LVDS, LVPECL & CML to LVDS buffer, repeater & translator
2	Texas Instruments	SN65LVDS1D	TI	SN65LVDS1DG4, LVDS Transmitter LVTTL Driver
1	Texas Instruments	SN65LVDT2D	TI	Single LVDS Receiver
5	Texas Instruments	SN74AVC4T245DGVR	Digi-Key	IC TRNSLTR BIDIREC-TIONAL 16TVSOP
2	Texas Instruments	SN74LVC1G11DCKR	Digi-Key	IC GATE AND 1CH 3-INP SC70-6
2	Texas Instruments	SN74LVC2G07DCKT	Digi-Key	IC BUF NON-INVERT 5.5V SC70-6
2	Texas Instruments	TCA6424ARGJR	Digi-Key	IC I/O EXPANDER I2C 24B 32UQFN
1	Texas Instruments	TCA9548APWR	Digi-Key	IC I2C SW 8CH W/RESET 24TSSOP
1	Texas Instruments	TCA9617ADGKR	Digi-Key	IC V-LEVEL XLATR FM+ I2C 8VSSOP
5	Texas Instrument	TCA9803	Digi-Key	IC V-LEVEL XLATR FM+ I2C 8VSSOP
2	Texas Instruments	TL1963A-33DCYR	Digi-Key	IC REG LINEAR 3.3V 1.5A SOT223-4
2	E-Switch	TL3301EF100QG	Digi-Key	SWITCH TACTILE SPST-NO 0.05A 12V
7	Texas Instruments	TMP435ADGSR	TI	DUAL TERMPERATURE SENSOR, 1REMOTE+1 INTERNAL
9	Keystone Electron-ics	5002	Digi-Key	PC TEST POINT MINIATURE White
2	Keystone Electron-ics	5002	Digi-Key	PC TEST POINT MINIATURE White
2	Texas Instruments	TPD4S012DRYR	Digi-Key	TVS DIODE 5.5V 6SON
1	Texas Instruments	TPS389001DSER	Digi-Key	IC SUPERVISOR 1 CHANNEL 6WSON

Table 3.12 continued from previous page

QTY	Manufacturer	Part Number	Distributor	Description
1	Texas Instruments	TPS51200DRCT	Digi-Key	IC REG CONV DDR 1OUT 10VSON
1	Texas Instruments	TPSM5601R5SRDAR	TI	4.2V TO 60V INPUT 1.5A 1V TO 6V 400KH SS
2	Eaton - Electronics Division	TR/3216FF3-R	Digi-Key	FUSE BRD MNT 3A 32VAC 63VDC 1206
2	DCT	USB4105-GF-A	Digi-Key	CONN RCP USB2.0 TYP C 24P SMD RA
1	TDK Corporation	VLS2012ET-6R8M	Digi-Key	TDK VLS-E Series Shielded Wire-wound SMD Inductor
8	Vishay Dale	WSK06125L000FEA	Digi-Key	CURRENT SENSE RESISTOR
1	Vishay Dale	WSL3637R0100FEA	Digi-Key	RES 0.01 OHM 1% 3W 3637
1	Xilinx	XCVM1802-1MSEVSVA2197	Avnet	IC ACAP 692 I/O VSVA2197
1	Abracon LLC	ABM8AIG-25.000MHZ-8-T	Digi-Key	CRYSTAL 25.0000MHZ 8PF SMD

3.9 Input/Output

3.9.1 Clock distribution

FLX-182 receives the BC clock from the LHC via the TTC system or generates the clock internally. To meet the GBT/lpGBT and GTY clock jitter requirements, Si5345 jitter attenuators [19] are used to clean the recovered clock from TTC system, and fanout to GTY reference clocks. Figure 3.26 shows the clock distribution on FLX-155.

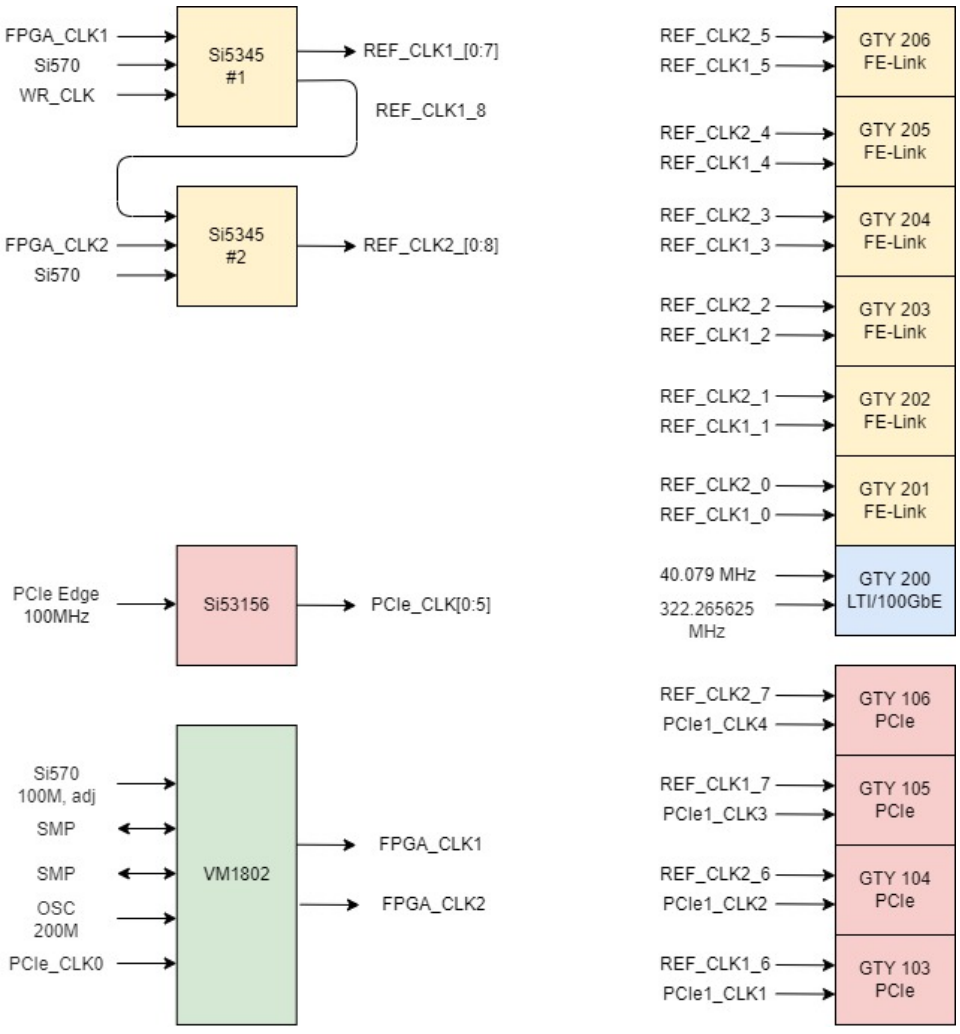


Figure 3.26: Block diagram of clock distribution on FLX-182.

3.9.2 Optical Data Links

FLX-182 hosts two ECUO-Y12 Firefly module TX/RX pairs, supporting 12 duplex links each. The ECUO-Y12 assembly is shown in Figure 3.27: a 24-fiber pigtail connects a TX and an RX module and terminates in a male MTP connector. The male MTP plug connects into the key-up to key-down coupler installed on the card front panel, as illustrated in Figure 3.28. The fiber mapping seen from outside the FLX-182 card is shown in Figure 3.29.

The ECUO-Y12 FireFly modules can either be ECUO-Y12-16 or CERN-B-Y12 for 10 Gb/s communication, or ECUO-Y12-25 rated for 25.7 Gb/s. In principle FLX-182 could host one ECUO-Y12-16 and one ECUO-

Y12-25 thus supporting 12 links at 10 Gb/s and 12 at 25 Gb/s, but no use case exists in ATLAS for such configuration.

The mapping between fibers and FPGA GTY transceivers (grouped in sets of four called Quads) is reported in Table 3.13, while the mapping between fibers and FPGA GTY pins is shown in Figures 3.30 to 3.33 and summarized in Figure 3.34. At least one out of the two reference clocks of each GTY Quad is connected to an output of two Si5345 jitter cleaner.

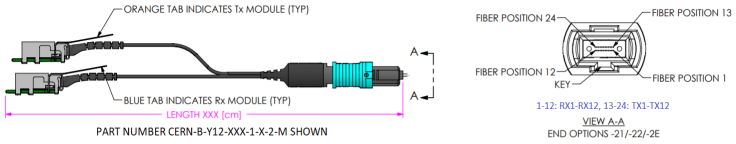
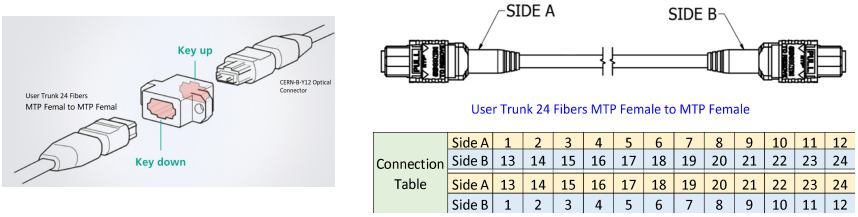


Figure 3.27: ECUO-Y12 optical connector pin out.



Connection Table												
	Side A	1	2	3	4	5	6	7	8	9	10	11	12
	Side B	13	14	15	16	17	18	19	20	21	22	23	24
	Side A	13	14	15	16	17	18	19	20	21	22	23	24
	Side B	1	2	3	4	5	6	7	8	9	10	11	12

Figure 3.28: Drawing of key-up to key-down coupler and MPO-24 user fiber. Left is the connection with key down and key up coupler. Right is the mapping of user trunk 24 fibers.

RX1	RX2	RX3	RX4	RX5	RX6	RX7	RX8	RX9	RX10	RX11	RX12
TX1	TX2	TX3	TX4	TX5	TX6	TX7	TX8	TX9	TX10	TX11	TX12
					KEY						

a. Channel 1-12

RX13	RX14	RX15	RX16	RX17	RX18	RX19	RX20	RX21	RX22	RX23	RX24
TX13	TX14	TX15	TX16	TX17	TX18	TX19	TX20	TX21	TX22	TX23	TX24
					KEY						

b. Channel 13-24

Figure 3.29: Mapping for ECUO-Y12 optical connector pins to the FLX-182 GTY channels, looking from outside of the MTP coupler after the ECUO-Y12 optical connector plugged in.

Table 3.13: Mapping for ECUO-Y12 optical connector pins to the FLX-182 GTY channels, with reference to the ECUO-Y12 optical connector (i.e., not the outward side of the coupler).

GTY Quad Ch.	FireFly link	GTY Quad Ch.	Firefly Link
Q201 : CH0	FireFly 1 : CH0	Q204 : CH0	FireFly 2 : CH0
Q201 : CH1	FireFly 1 : CH1	Q204 : CH1	FireFly 2 : CH1
Q201 : CH2	FireFly 1 : CH2	Q204 : CH2	FireFly 2 : CH2
Q201 : CH3	FireFly 1 : CH3	Q204 : CH3	FireFly 2 : CH3
Q202 : CH0	FireFly 1 : CH4	Q205 : CH0	FireFly 2 : CH4
Q202 : CH1	FireFly 1 : CH5	Q205 : CH1	FireFly 2 : CH5
Q202 : CH2	FireFly 1 : CH6	Q205 : CH2	FireFly 2 : CH6
Q202 : CH3	FireFly 1 : CH7	Q205 : CH3	FireFly 2 : CH7
Q203 : CH0	FireFly 1 : CH8	Q206 : CH0	FireFly 2 : CH8
Q203 : CH1	FireFly 1 : CH9	Q206 : CH1	FireFly 2 : CH9
Q203 : CH2	FireFly 1 : CH10	Q206 : CH2	FireFly 2 : CH10
Q203 : CH3	FireFly 1 : CH11	Q206 : CH3	FireFly 2 : CH11

TX: From FELIX
RX: To FELIX

Channel	RX_P	Channel	RX_P	Channel	RX_P	Channel	RX_P	Channel	RX_P	Channel	RX_P
1	AB2	5	V2	9	P2	13	K2	17	G4	21	D2
2	AA4	6	U4	10	N4	14	J4	18	F2	22	D6
3	Y2	7	T2	11	M2	15	H2	19	F6	23	C4
4	W4	8	R4	12	L4	16	H6	20	E4	24	B6
Channel	TX_P	Channel	TX_P	Channel	TX_P	Channel	TX_P	Channel	TX_P	Channel	TX_P
1	AB7	5	V7	9	P7	13	K7	17	G9	21	C9
2	AA9	6	U9	10	N8	14	K11	18	F11	22	B11
3	Y7	7	T7	11	M7	15	J9	19	E9	23	A9
4	W9	8	R9	12	L9	16	H2	20	D11	24	A13

Figure 3.30: Mapping for ECUO-Y12 optical connector pins to FLX-182 GTY pins.

KEY

AB2	AA4	Y2	W4	V2	U4	T2	R4	P2	N4	M2	L4
AB7	AA9	Y7	W9	V7	U9	T7	R9	P7	N8	M7	L9

a. Channel 1-12

KEY

K2	J4	H2	H6	G4	F2	F6	E4	D2	D6	C4	B6
K7	K11	J9	H2	G9	F11	E9	D11	C9	B11	A9	A13

b. Channel 13-24

Figure 3.31: Mapping for ECUO-Y12 optical connector pins to FLX-182 GTY pins, with reference to the ECUO-Y12 optical connector.

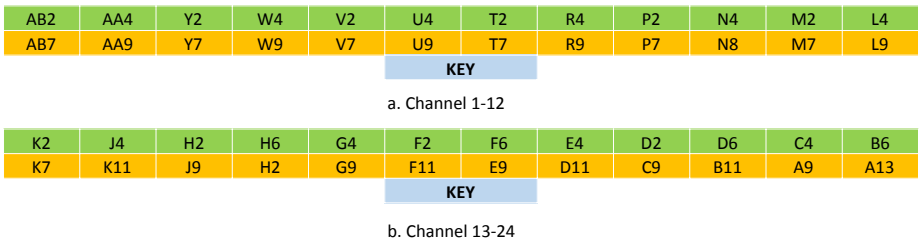


Figure 3.32: Mapping for ECUO-Y12 optical connector pins to FLX-182 GTY pins, looking from outside of the MTP coupler after the ECUO-Y12 optical connector plugged in.

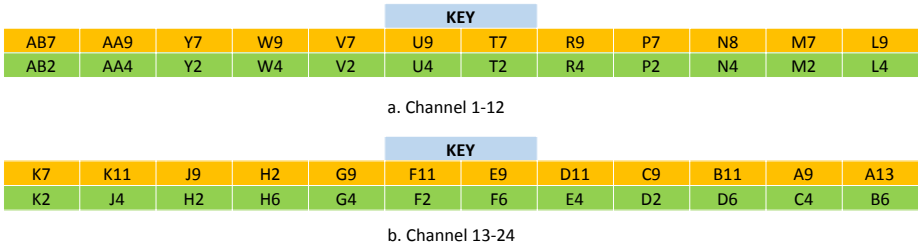


Figure 3.33: Mapping for user fiber to FLX-182 GTY pins, looking from near end (close to FLX-182) of user trunk fiber.

Fiber Channel	MTP Couple	User Fiber (Female, Near end)	MTP Coupler Pin (*)	CERN-B-Y12 Optical Connector Pin (Male)	CERN-B-Y12	CERN-B-Y12 Channel	FLX-182 Pin (P end)
TX1	1	1	12	13	J29 TX	TX-0	AB7
TX2	1	2	11	14	J29 TX	TX-1	AA9
TX3	1	3	10	15	J29 TX	TX-2	Y7
TX4	1	4	9	16	J29 TX	TX-3	W9
TX5	1	5	8	17	J29 TX	TX-4	V7
TX6	1	6	7	18	J29 TX	TX-5	U9
TX7	1	7	6	19	J29 TX	TX-6	T7
TX8	1	8	5	20	J29 TX	TX-7	R9
TX9	1	9	4	21	J29 TX	TX-8	P7
TX10	1	10	3	22	J29 TX	TX-9	N8
TX11	1	11	2	23	J29 TX	TX-10	M7
TX12	1	12	1	24	J29 TX	TX-11	L9
RX1	1	13	24	1	J22 RX	RX-0	AB2
RX2	1	14	23	2	J22 RX	RX-1	AA4
RX3	1	15	22	3	J22 RX	RX-2	Y2
RX4	1	16	21	4	J22 RX	RX-3	W4
RX5	1	17	20	5	J22 RX	RX-4	V2
RX6	1	18	19	6	J22 RX	RX-5	U4
RX7	1	19	18	7	J22 RX	RX-6	T2
RX8	1	20	17	8	J22 RX	RX-7	R4
RX9	1	21	16	9	J22 RX	RX-8	P2
RX10	1	22	15	10	J22 RX	RX-9	N4
RX11	1	23	14	11	J22 RX	RX-10	M2
RX12	1	24	13	12	J22 RX	RX-11	L4
TX13	2	1	12	13	J28 TX	TX-0	K7
TX14	2	2	11	14	J28 TX	TX-1	K11
TX15	2	3	10	15	J28 TX	TX-2	J9
TX16	2	4	9	16	J28 TX	TX-3	H2
TX17	2	5	8	17	J28 TX	TX-4	G9
TX18	2	6	7	18	J28 TX	TX-5	F11
TX19	2	7	6	19	J28 TX	TX-6	E9
TX20	2	8	5	20	J28 TX	TX-7	D11
TX21	2	9	4	21	J28 TX	TX-8	C9
TX22	2	10	3	22	J28 TX	TX-9	B11
TX23	2	11	2	23	J28 TX	TX-10	A9
TX24	2	12	1	24	J28 TX	TX-11	A13
RX13	2	13	24	1	J21 RX	RX-0	K2
RX14	2	14	23	2	J21 RX	RX-1	J4
RX15	2	15	22	3	J21 RX	RX-2	H2
RX16	2	16	21	4	J21 RX	RX-3	H6
RX17	2	17	20	5	J21 RX	RX-4	G4
RX18	2	18	19	6	J21 RX	RX-5	F2
RX19	2	19	18	7	J21 RX	RX-6	F6
RX20	2	20	17	8	J21 RX	RX-7	E4
RX21	2	21	16	9	J21 RX	RX-8	D2
RX22	2	22	15	10	J21 RX	RX-9	D6
RX23	2	23	14	11	J21 RX	RX-10	C4
RX24	2	24	13	12	J21 RX	RX-11	B6

Figure 3.34: Full Mapping of FLX-182 FireFly Optical Fibers to GTY Links, looking from outside of the MTP coupler after the ECUO-Y12 Optical Connector plugged in.

3.9.3 LTI Optical Interface or 100 GbE

An ECUO-B04 FireFly module, with four transmitter and four receiver channels, is used for the LTI interface (or 100 GbE). The eight fibers are bundled in an MTP-12 connector, as shown in Figure 3.35. The signal mapping on MTP-12 is shown in Figure 3.36. All ECUO-B04 channels connect to GTY Quad 200 that is provided with two reference clocks at 40.079 MHz and 322.265 625 MHz from the respective oscillators.

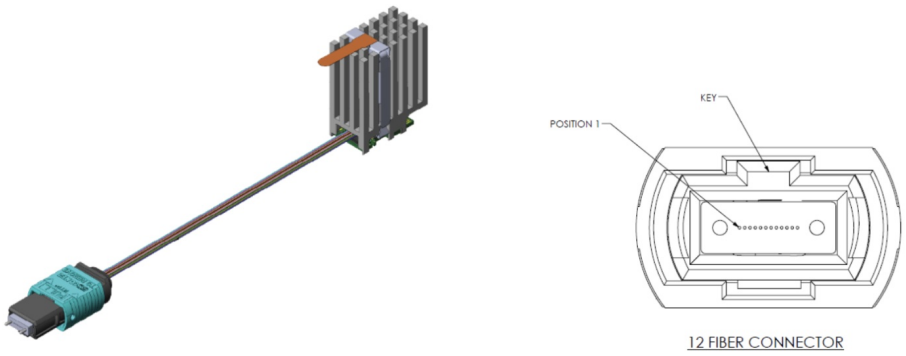


Figure 3.35: ECUO-B04 4-ch optical connector pin out.

SIGNAL MAP				
LOAD SEQUENCE	FUNCTION	COLOR		MTP POSITION
1	Rx0	BLUE		1
2	Rx1	ORANGE		2
3	Rx2	GREEN		3
4	Rx3	BROWN		4
5	Dark	SLATE		5
6	Dark	WHITE		6
7	Dark	RED		7
8	Dark	BLACK		8
9	Tx4	YELLOW		9
10	Tx3	VIOLET		10
11	Tx2	ROSE		11
12	Tx1	AQUA		12

Figure 3.36: Signal map of MTP-12 for ECUO-B04 4-ch optical connector.

3.9.4 PCIe interface

On VM1802 the PCIe interface can be implemented using either the PL (as in the Phase-I FELIX implementation) or the CPM core available on Versal devices [**PCI_PCI_CPM**, 20]. The PL implementation supports up to four Gen4×8 links, CPM supports one Gen4×16 or two Gen4×8 and has a hard connection to the network-on-chip (NOC). Both options are currently supported by FELIX firmware and have been tested. In both cases, GTY Quads 103 to 106 are used. Each Quad receives one reference clock from an output of the Si53156 clock buffer, and one from the PCIe bus 100 MHz clock. The mapping of GTY PCIe channels is shown in Table 3.14.

Table 3.14: Mapping of GTY and PCIe channels.

GTY Quad: CH	Link
Q103 : Ch0	PCIe Ch0
Q103 : Ch1	PCIe Ch1
Q103 : Ch2	PCIe Ch2
Q103 : Ch3	PCIe Ch3
Q104 : Ch0	PCIe Ch4
Q104 : Ch1	PCIe Ch5
Q104 : Ch2	PCIe Ch6
Q104 : Ch3	PCIe Ch7
Q105 : Ch0	PCIe Ch8
Q105 : Ch1	PCIe Ch9
Q105 : Ch2	PCIe Ch10
Q105 : Ch3	PCIe Ch11
Q106 : Ch0	PCIe Ch12
Q106 : Ch1	PCIe Ch13
Q106 : Ch2	PCIe Ch14
Q106 : Ch3	PCIe Ch15

3.9.5 DDR4 MEMORY

The XPIO I/O banks of VM1802 are specifically designed to support the signals to and from the external DDR memories. The I/O banks can use the XPHY to align, serialize, and de-serialize a data stream. Each I/O bank has nine nibbles of six cells each for a total of 54 pins. The input and output buffers support a wide range of single-ended and differential I/O standards along with resources to support a high level of signal quality. Each buffer has I/O interconnect logic resources to support low-speed SDR and DDR memory interfaces and coarse data alignment resources. One DDR4 Mini-UDIMM w/ ECC slot is available on FLX-182, which can support 16GB DDR4 module connected to XPIO Bank 703-705. The part-number of the DDR4 Mini-UDIMM is Innodisk M4M0-AGS1YCSJ (PC4-2400) and has been verified on an earlier prototype card called FLX-181

3.9.6 ETHERNET

A PS Gigabit Ethernet MAC (GEM) implements a 10/100/1000 Mb/s Ethernet interface (Table 3.15), which connects to TI DP83867ISRGZ Ethernet RGMII PHY [21] before being routed to a RJ45 Ethernet connector. The RGMII Ethernet PHY is boot-strapped to PHY address (0x01) and Auto Negotiation is enabled.

3.9.7 ELECTRICAL TRIGGER INTERFACE

The FLX-182 bracket hosts six MMCX connectors that can be used to implement a trigger interface. Two input connectors can be used for clock and trigger while one output can rout the legacy BUSY signal. The remaining input and two outputs are reserved for BCM' use.

The trigger signal input, which is compatible with the ALTI interface, uses NIM logic. It is converted into LVPECL by ADCMP561 [22], then to LVDS by SN65LVDS100 [23], and sent to FPGA. Figure 3.37 shows the connection of the route.

3.9.8 WHITE RABBIT

The White Rabbit (WR) project [24] is a timing control solution that aims at synchronizing over 1000 nodes with sub-nanosecond accuracy over fiber lengths of up to 10 km. FLX-182 is designed to be a compliant WR node. VM1802 is used to implement the WR PTP Core (WRPC). VCXOs and DACs are used to generate reference clock and MTD clock, as shown in Figure 3.38. A four-channel FireFly module is used for WR

Table 3.15: Pin mapping of GEM0 Ethernet.

LPD 502 MIO bank pin	RGMII signals
0	GTX_CLK
1	TX_D0
2	TX_D1
3	TX_D2
4	TX_D3
5	TX_CTRL
6	RX_CLK
7	RX_D0
8	RX_D1
9	RX_D2
10	RX_D3
11	RX_CTRL
24	MDC
25	MDIO

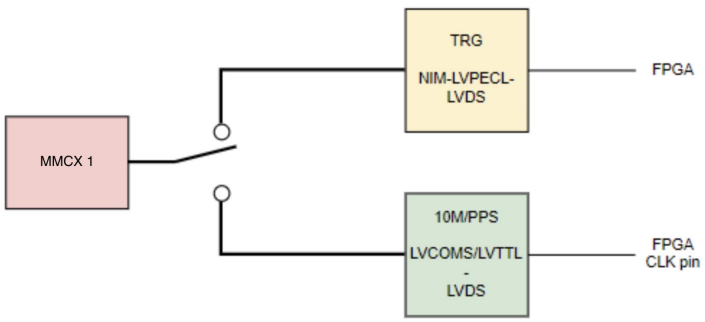


Figure 3.37: Electrical signal of TTC trigger on FLX-182.

link. Two MMCX connectors on front panel, J11 and J51, can be used for WR PPS and 10 MHz clock input. J11 can be configured to be as TTC electrical trigger input, or WR clock input by populating different resistor jumpers. An SMP connector J10 is used as PPS output for performance measurement.

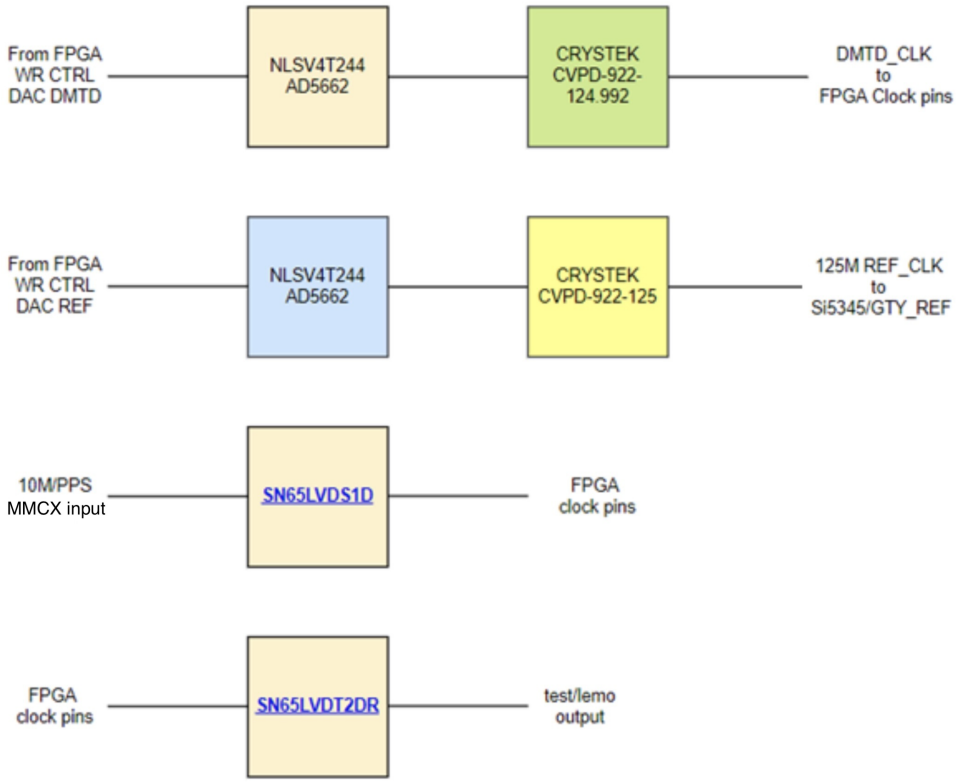


Figure 3.38: Interface mapping for the White Rabbit protocol.

3.10 Control and Monitoring

3.10.1 I2C bus

The I2C bus is used to monitor voltages, currents and temperatures, as well as the optical power of FireFly transceivers. Four controller nodes are connected to the I2C bus: the PS (via bank 501), PL (via HDIO bank 406), the USB-to-I2C converter FT4232 used for the USB-C port on the front panel, and, optionally, the SMBUS on PCIe edge. In the last revision, the SMBUS interface has been disconnected to avoid possible address conflicts on the host server and not to rely on the limited motherboard support. The controllers are interfaced with the eight-channel switch TCA9548A as shown in Figure 3.39. The devices connected to each channel are shown in Figure 3.40. Device addresses are listed in 3.16.

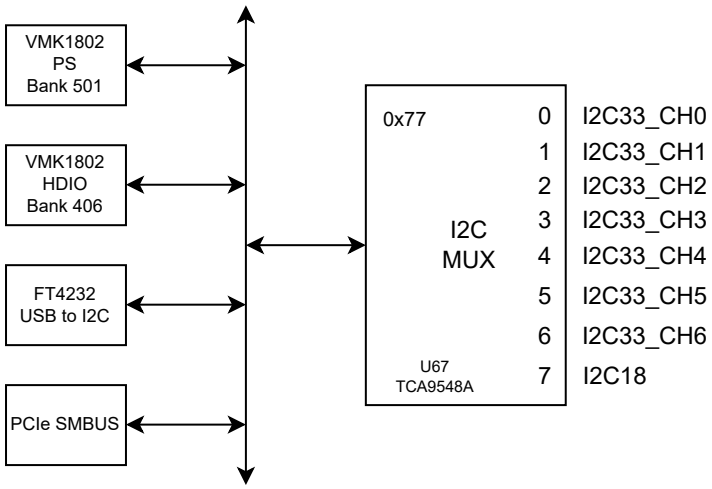


Figure 3.39: Overview of the I2C bus connections.

3.10.2 Firmware storage, update and debugging

Multiple firmware images can be stored on the secure digital (SD) card or Quad-SPI (QSPI) flash memory. The default storage device is configured using the DIP switch using the settings listed in Table 3.17.

The PS has access to the I2C bus and the SD card. Therefore software running on the PS can manage firmware images on both the SD cards and the flash memory. In addition, monitoring information can be retrieved from the I2C bus and shared over the network. Either a virtual network interface implemented over PCIe or the physical one can be used to share the monitoring data.

For debugging purposes, Xilinx Virtual Cable [25] can be run on PS and reached via the physical (or a virtual) network interface.

3.10.2.1 SD Card

An SD card is provided for booting and file system storage. This interface is used for the SD boot mode and supports SD3.0 access. To boot from the SD card:

1. Store a valid XCVM1802 ACAP boot image file on a microSD card. Insert the SD card into the FLX-182 board SD socket J52.
2. Set boot MODE U24 for SD_3.0 as indicated in c3.17.
3. Power-cycle the FLX-182.

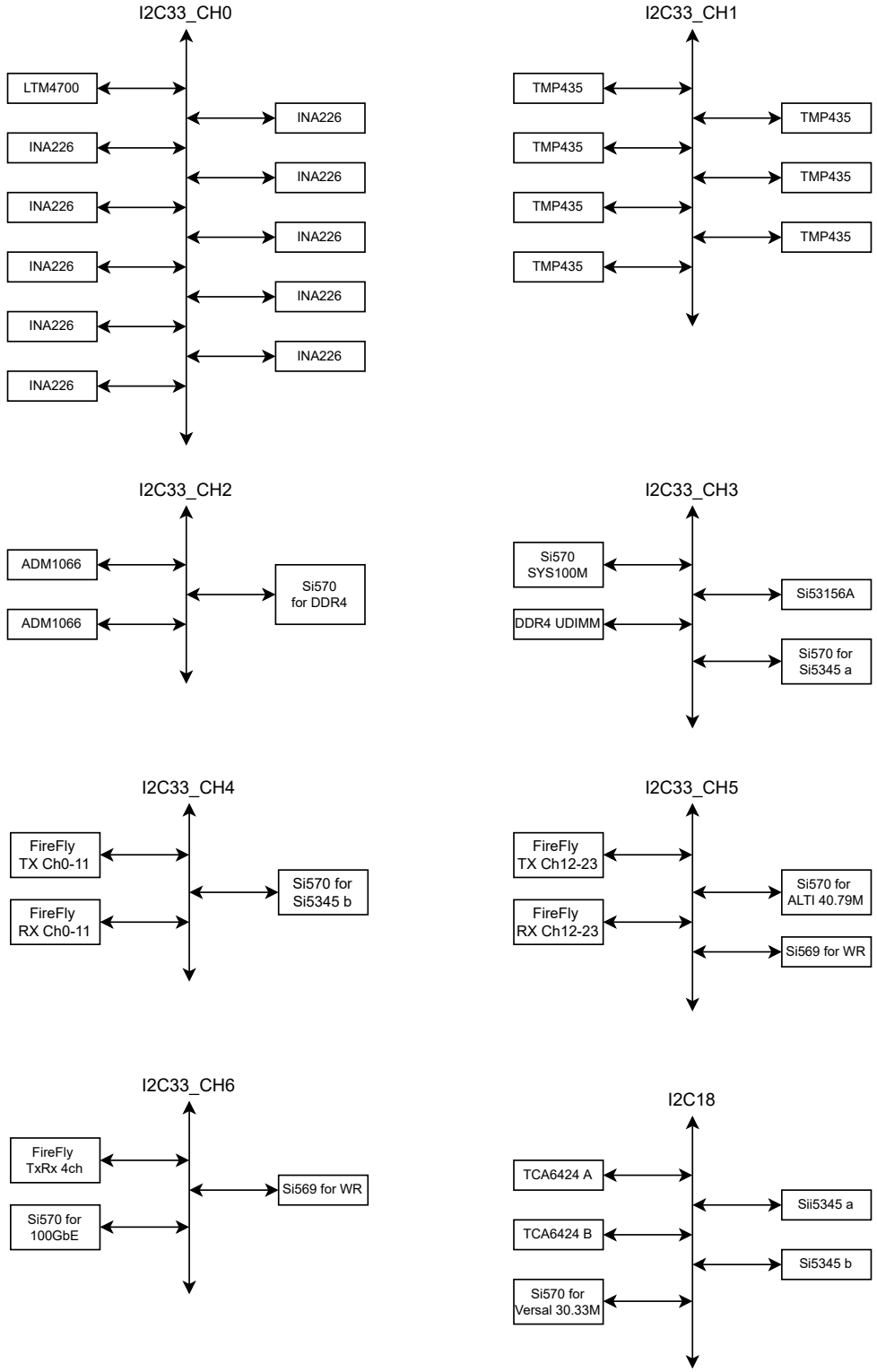


Figure 3.40: I2C bus connections of I2C switch TCA9548A.

Table 3.16: I2C addresses on FLX-182.

Item	Category	Part	Description	I2C BUS name	Address	Voltage
1	pwr module	LTM4700	PWR_VCCINT	I2C33_CH0	0X4E	3.3
2	pwr v/i	INA226	12P0V	I2C33_CH0	0X40	3.3
3	pwr v/i	INA226	VCCINT	I2C33_CH0	0X41	3.3
4	pwr v/i	INA226	MGTAVCC	I2C33_CH0	0X42	3.3
5	pwr v/i	INA226	MGTAVTT	I2C33_CH0	0X43	3.3
6	pwr v/i	INA226	SYS12	I2C33_CH0	0X44	3.3
7	pwr v/i	INA226	SYS15	I2C33_CH0	0X45	3.3
8	pwr v/i	INA226	SYS18	I2C33_CH0	0X46	3.3
9	pwr v/i	INA226	SYS25	I2C33_CH0	0X47	3.3
10	pwr v/i	INA226	SYS33	I2C33_CH0	0X48	3.3
11	pwr v/i	INA226	SYS38	I2C33_CH0	0X49	3.3
12	pwr tmp	TMP435	MGTAVCC	I2C33_CH1	0x48	3.3
13	pwr tmp	TMP435	MGTAVTT	I2C33_CH1	0x49	3.3
14	pwr tmp	TMP435	SYS12	I2C33_CH1	0x4A	3.3
15	pwr tmp	TMP435	SYS15	I2C33_CH1	0x4B	3.3
16	pwr tmp	TMP435	SYS18	I2C33_CH1	0x4C	3.3
17	pwr tmp	TMP435	SYS33	I2C33_CH1	0x4D	3.3
18	pwr tmp	TMP435	LTM4642(sys25/38)	I2C33_CH1	0x4E	3.3
19	clock	SI570	versal_ref_clk, 30.33MHz	I2C18	0x5D	1.8
20	clock	SI570	sys100M	I2C33_CH3	0x55	3.3
21	clock	SI570	DDR4 clock, 200MHz	I2C33_CH2	0x60	3.3
22	clock	si570	si5345 a in1 clock 40.079M	I2C33_CH3	0x60	3.3
23	clock	si570	si5345 b in1 clock 40.079M	I2C33_CH4	0x60	3.3
24	clock	Si570	LTI refclk for GTY 40.079M	I2C33_CH5	0x60	3.3
25	clock	si570/Si540	100G refclk for GTY 322.265625M	I2C33_CH6	0x60	3.3
26	clock	si5345	si5345 a	I2C18	0x68	1.8
27	clock	si5345	si5345 b	I2C18	0x69	1.8
28	clock	si53156A	pcie clock fan out	I2C33_CH3	0xd6	3.3
29	FireFly	FF12 TX	FF12 Ch0-11 TX	I2C33_CH4	0x50	3.3
30	FireFly	FF12 RX	FF12 Ch0-11 RX	I2C33_CH4	0x54	3.3
31	FireFly	FF12 TX	FF12 Ch12-23 TX	I2C33_CH5	0x50	3.3
32	FireFly	FF12 Rx	FF12 Ch12-23 RX	I2C33_CH5	0x54	3.3
33	FireFly	FF4 TRx	FF4 TX/RX	I2C33_CH6	0x50	3.3
34	ADM1066	ADM1066	pwr management	I2C33_CH2	0x34	3.3/3.3_aux
35	ADM1066	ADM1066	pwr management	I2C33_CH2	0x35	3.3/3.3_aux
36	DDR4	DDR4 MINIDIMM	DDR4	I2C33_CH3	0x53	3.3
37	I2C IO extender	TCA6424A	IO extender	I2C18	0x22	1.8
38	I2C IO extender	TCA6424A	IO extender	I2C18	0x23	1.8
39	WR_OSC	SI569	OSC for WR	I2C33_CH5	0x55	3.3
40	WR_OSC	SI569	OSC for WR	I2C33_CH6	0x55	3.3

Table 3.17: Boot mode configuration settings on DIP switch U24.

Boot Mode	Mode[3:0]	DIP switch U24 position [4:1]
JTAG	0000	ON, ON, ON, ON
QSPI32	0010	ON, ON, OFF, ON
SD1_3.0	1110	OFF, OFF, OFF, ON

3.10.2.2 QSPI Flash

Two QSPI Flash MT25QU02GC devices are connected to XCVM1802 U2 bank 500 PMC_MIO [0:5, 7:12] pins. The supported QSPI configurations are x1, x2, x4, and dual-parallel x8. To boot from a QSPI device:

1. Store a valid VM1802 boot image file to the QSPI device.
2. Set boot mode U24 for QSPI32 as indicated in Table 3.17.
3. Power-cycle the FLX-182.

3.10.2.3 JTAG

FLX-182 has two physical JTAG interfaces.

- Digilent USB-to-JTAG device (U57) connected to micro-USB connector (J46).
- JTAG pod flat cable connector J47 (2 mm 2x7 shrouded/keyed).

Either J46 or J47 can be used to program the XCVM1802 through JTAG, provided that the DIP switch U24 is set in JTAG mode as indicated in Table 3.17.

3.10.3 Power on Reset

Versal ACAP Technical Reference Manual (AM011): The active-Low POR_B pin is the global power-on reset for the Versal ACAP. POR_B must remain asserted Low until power is fully applied to at least the VCC_PMC, VCCAUX_PMC, and VCCO_503. When the reset is released, the PMC begins the initialization and boot process. To meet the requirement, 1.5 V power rail is monitored by TPS3890. When the power rail exceeds the threshold, the POR_B will be released after delay, which can be configured by the timing capacitor C313. There are five other signals can be optionally used to control POR_B.

- Push-button SW1: must be released to release POR_B
- JTAG_CON_SRST_B (optional)
- USB_JTAG_SRST_B (optional)
- ALL_PWR_GOOD from ADM1066 (optional)
- I2C_GPIO_POR (optional), can be used to trigger the VM1802 reprogramming through I2C bus

3.11 Integration tests

At the present time less than 10 samples of FLX-182 exist and they are in the hand of institutes involved in Readout. Widespread integration tests will be carried out in 2024 when about 36 FLX-182 samples will be distributed to sub-detector teams. Nevertheless representative integration tests have been carried out with FLX-182. The most important test hardware-wise was the validation of 25 Gb/s communication, carried out with Global Trigger (GCMv2 board).

3.11.1 Integration with Global Trigger

The communication between FELIX (FLX-182) and Global Trigger (GCM) has been tested in February 2023 at BNL. In this test, the uplink is rated at 25.781 25 Gb/s and uses the Interlaken protocol. The 8b10b-encoded 9.6 Gb/s downlink is used to relay LTI messages. LTI messages were then received and parsed by Global (Figure 3.41). No errors were observed in a short PRBS31 test on the downlink corresponding to a bit-error rate $< 6.7 \times 10^{-14}$. An open eye test reported an area > 5486 on all the eight links test (Figure 3.42). The Core1990 [2] gearbox in FELIX aligned and the correct header and sync words where observed using an ILA probe (Figure 3.43).

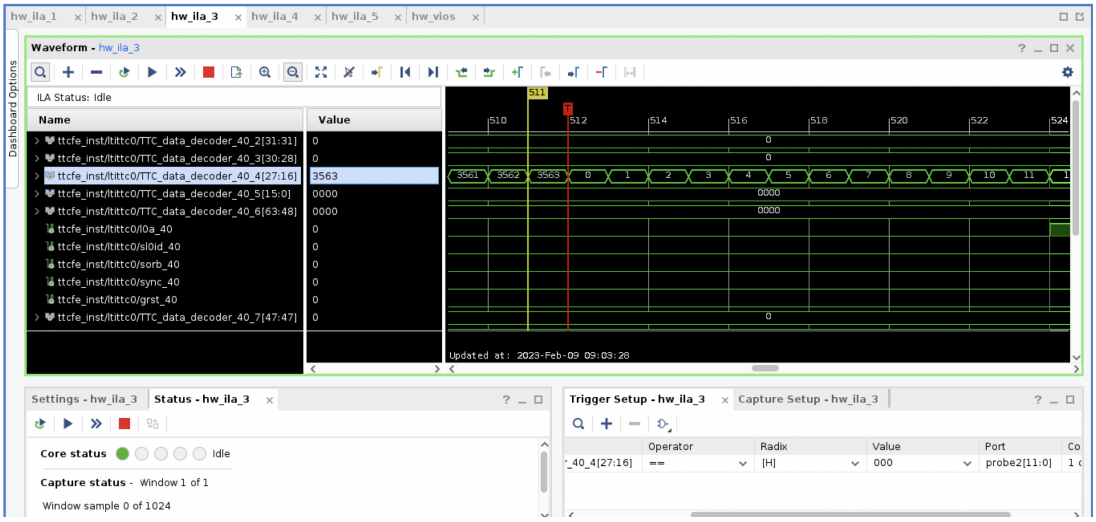


Figure 3.41: LTI messages received by GCMv2.

3.11.2 Integration with LTI

In order to test the communication with LTI in the absence of an LTI hardware prototype, the NIKHEF team developed an LTI emulator on a development board [27, 28]. The board is Enclustra Mercury+ ST1 equipped with a Mercury+ XU1 system-on-module and an SFP+ FMC module. Both uplink and downlink communication has been demonstrated with a FLX-182. The test did not include the demonstration of pico-second phase stability, discussed in Chapter 4.

3.11.3 LpGBT and FULL links

For firmware and low-level software development purposes FLX-182 is regularly interfaced with a VLDB+ board. Similarly, FLX-182 is often connected to a FLX-712 that acts as FULL front-end board thanks to a dedicated firmware.

[2] Core1990 [26] is the open-source core that implements the Interlaken protocol in PL

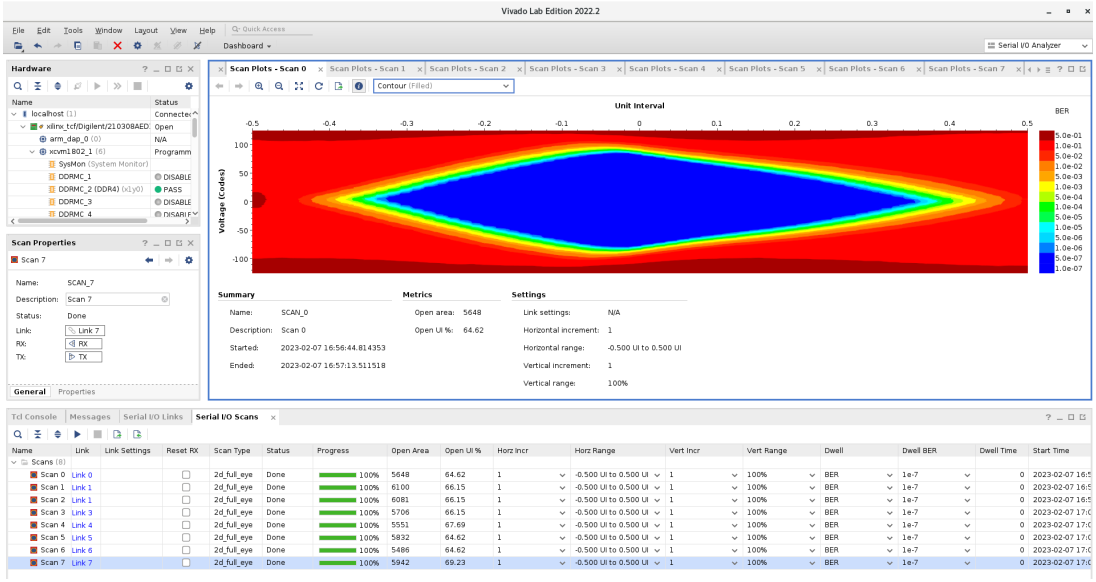


Figure 3.42: Open eye diagram measured on FLX-182 during the FELIX/Global integration test.

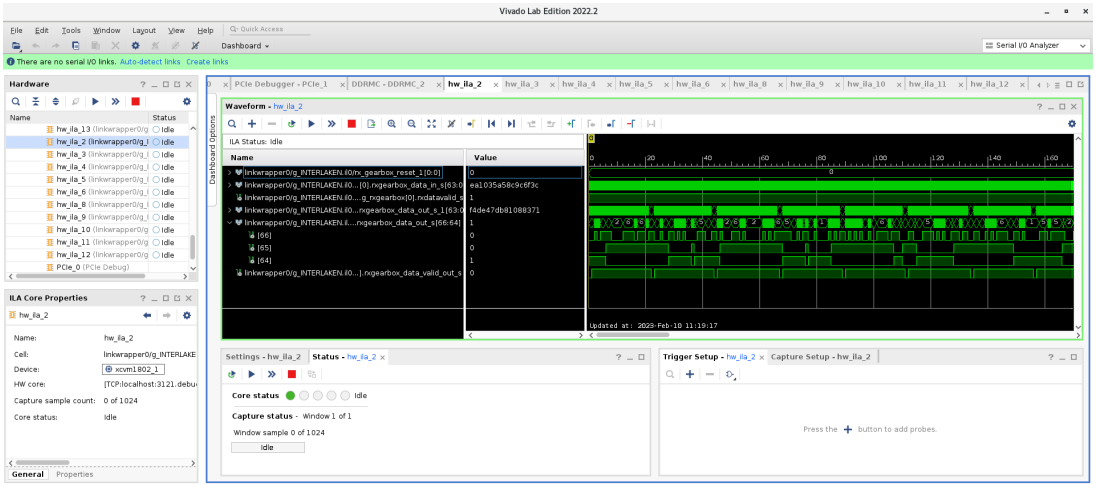


Figure 3.43: Probe of Interlaken data link on FLX-182 during the FELIX/Global integration test. The expected header and sync words are observed.

4

TIMING DISTRIBUTION WITH TCLINK

The 40.079 MHz bunch clock (BC) must be distributed with arbitrary but fixed and deterministic phase. The BC distribution in ATLAS is illustrated in Figure 4.1. The BC is retrieved by the Central Trigger Processor (CTP) from the LHC-RF interface module and passed to LTI modules. Each LTI module is connected to multiple FELIX cards that relay the signal to detector electronics (actual front-ends or ATCA boards). The overall latency drifts, from CTP to front-end, must be smaller than 30 ps [29].

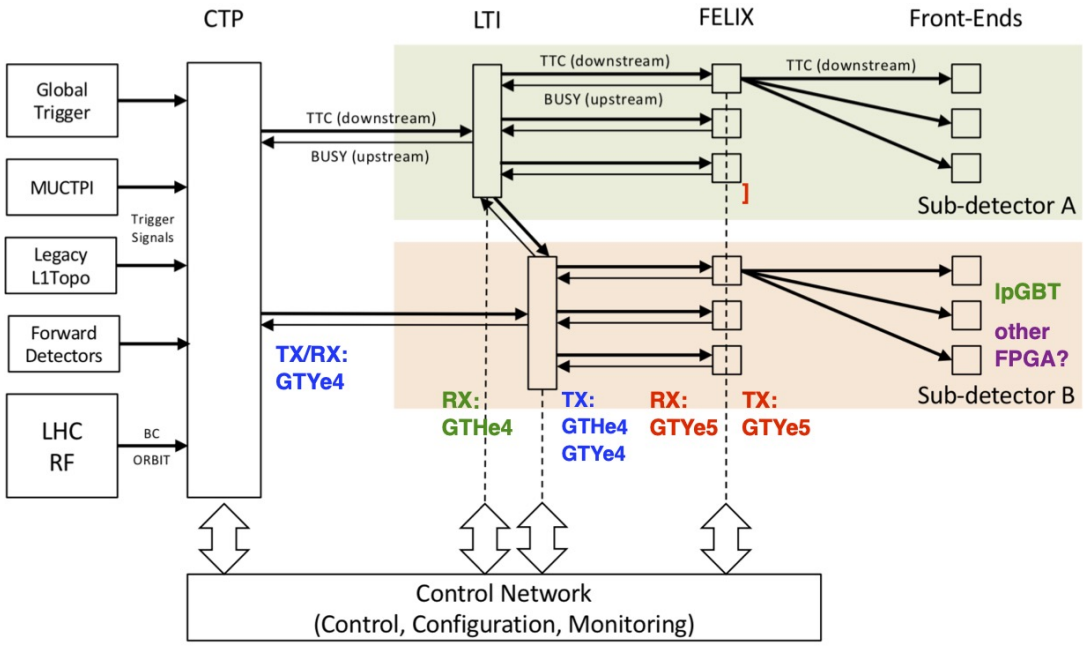


Figure 4.1: TTC distribution diagram.

4.1 TCLINK

TCLink [30] is a protocol-agnostic IP core designed to mitigate long-term phase variations in high-speed optical links. Considering a system composed of two nodes connected by a bi-directional link, the mechanism is based on the compensation of phase differences by one of the nodes, identified as master. The master

node transmits information to a slave node in the downlink direction and the slave node uses the recovered clock for the uplink transmission. The master node contrasts round-trip time variations by shifting the TX signal phase. TCLink can maintain phase variations below 10 ps for temperature variations of the optical fibers as large of 50 ℃ ensuring a phase stability within the HGTD requirement of 30 ps even for multiple hops across a master-slave chain.

However, The TCLink compensation mechanism alone cannot ensure phase determinism across node resets. Assuming both master and slave are FPGAs, phase determinism across resets can be achieved on the transmitting side implementing the HPTD IP core. HPTD uses the occupancy of an elastic FIFO to synchronize the TX reference clock and the TX serial data clock. On the receiving side, the recovered clock must have a predictable phase with respect to the byte boundary in the incoming serial stream. Either the recovered clock is shifted until serial stream header matches with the recovered clock (using the RXSLIDE signal) or the transceiver is reset until the two match (roulette approach) [31]. Both RXSLIDE and roulette approaches provide sub-UI phase stability within tens of ps [32].

4.1.1 RX PHASE DETERMINISM

The phase determinism across resets on the receiving side can be reduced acting on the transceivers parameters.

4.1.1.1 GTHE4

On AMD/Xilinx GTHe4 transceivers, used by the Ultrascale FPGA family, the phase uncertainty can be as low as a few ps if the automatic tuning of the receiver equalizer is disabled.

4.1.1.2 GTYE4

The approach used for GTHe4 leads to a wider phase spread for GTYe4 transceivers used by the Ultrascale+ FPGA family. The phase distribution for GTYe4s across resets is bi-modal as shown in Figure 4.2. In order to exclude one of the two peaks, the CTP Team devised a strategy that requires:

1. The injection of clock-like patterns in the data transmitted by the master;
2. A fan-out chip to pass data from the FireFly module to both the GTY transceiver and a phase detector. The phase detector measures the difference between the fan-out clock pattern and the RX user clock.
3. A simple algorithm implemented in software that commands a GTY reset until the phase falls in the selected peak.

4.1.1.3 GTYE5

The phase distribution originally obtained by the CTP team with GTYe5 transceivers used by the Versal FPGA family is multi-modal (Figure 4.2) and covers a range of about 40 ps. Tuning transceiver parameters, the FELIX team managed to obtain the bi-modal distribution shown in Figure 4.3, equivalent to the GTYe4 one. A strategy to consistently select the same phase, possibly without hardware modifications, is currently being devised.

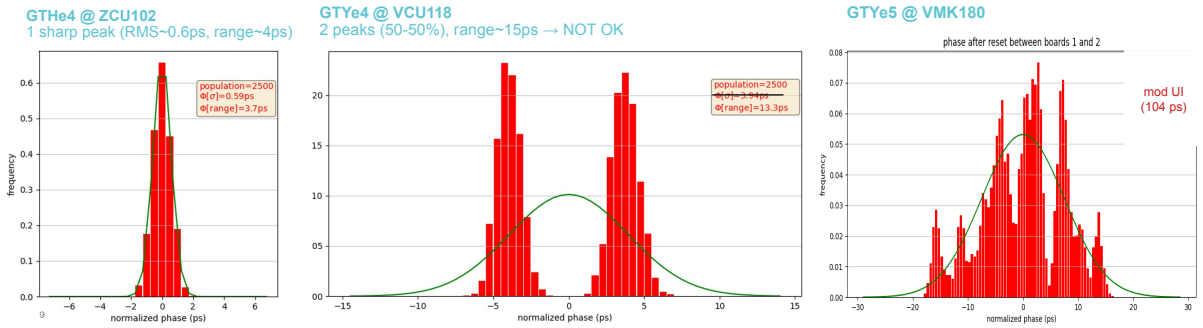


Figure 4.2: Comparison of RX phase distribution for GTH, GTYe4 and GTYe5 after reset. Presented by F. Bonini at the LTI PDR https://indico.cern.ch/event/1317854/.

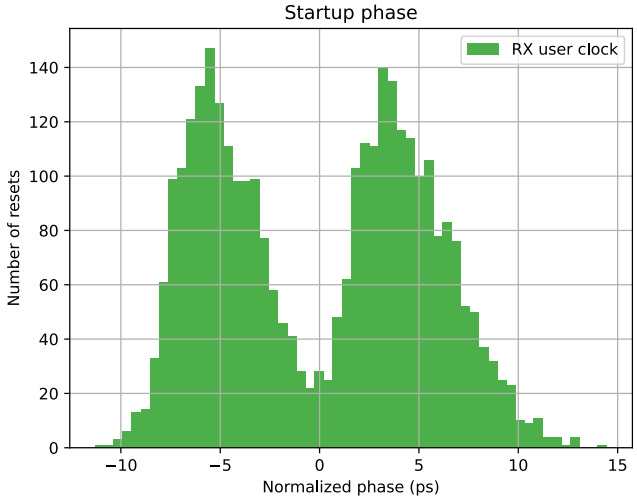


Figure 4.3: Phase of the RX clock recovered by FLX-182 across multiple resets.

4.1.2 TX PHASE DETERMINISM

The use of HPTD core ensures phase determinism for all transceiver types listed above. This has been demonstrated also using an FLX-182 (master) and a VLDB+ board (slave). Two clock signals are extracted from FLX-182 as illustrated in Figure 4.4: the GTYe5 TXUSERCLK and MGTREFCLK. The latter is used as trigger on the oscilloscope. The eCLK0 clock recovered by lpGBT and used for lpGBT ink 0 is also connected to the oscilloscope. Two latencies are measured across resets of the FLX-182 transmitter: TXUSERCLK – MGTREFCLK and eCLK0 – MGTREFCLK. The results are shown in Figure 4.5: the RMS for all three measurements is about 2 ps.

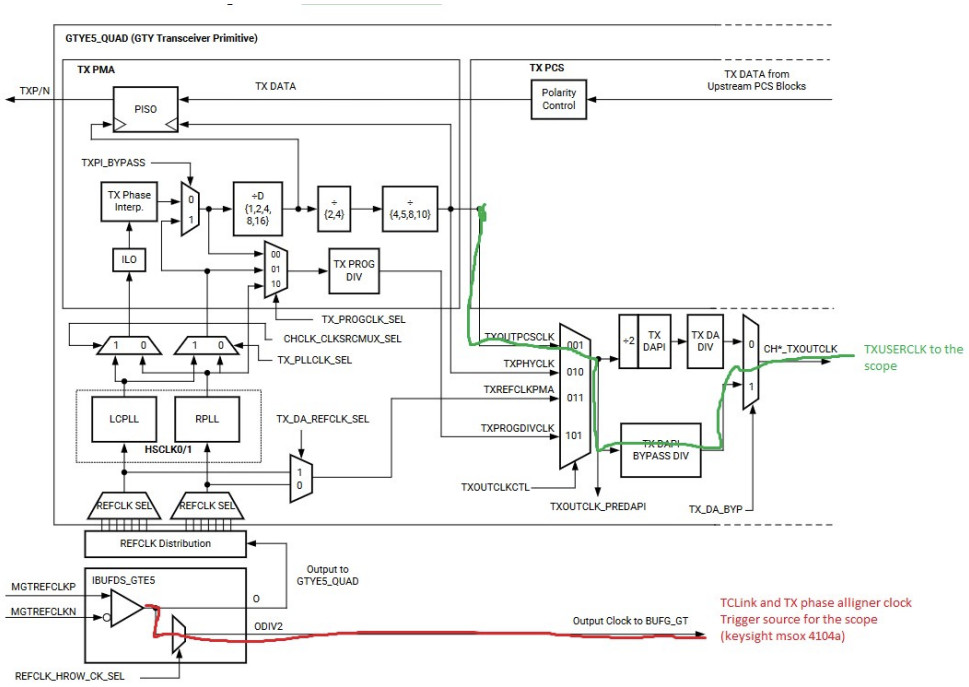


Figure 4.4: Clock signals extracted from GTYe5 transmitter on FLX-182.

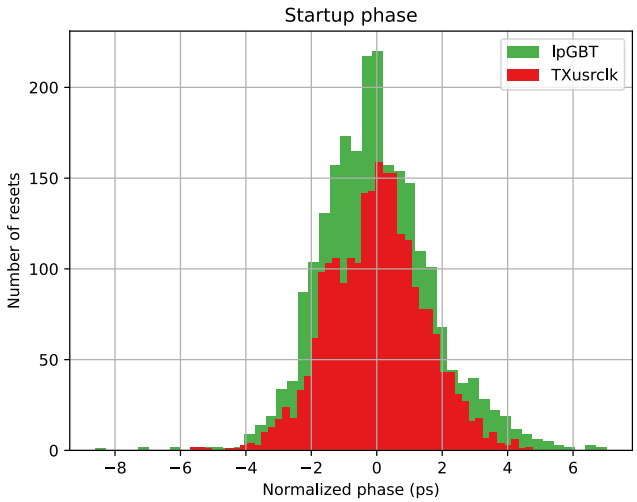


Figure 4.5: Measured latencies between clock signals. TXUSERCLK: phase of TXUSERCLK with respect to MGTREFCLK; lpGBT: phase between lpGBT's eCLK0 and MGTREFCLK.

4.2 Timing distribution chain

Figure 4.1 shows the transceiver type at each hop of the TTC system. Phase stability can currently be achieved on the CTP-LTI hop, and on the FELIX transmission side, both on the LTI-FELIX and the FELIX-FE hop. A solution is being sought after for the receiver of LTI information on FELIX. Two possible outcomes can be anticipated:

1. Modifications in FELIX firmware suffice.
2. An extra fiber has to be used to deliver a clock signal from LTI to FELIX. In this case firmware modification require FELIX hardware support. FLX-155 supports this option thanks to an additional electrical route from the LTI FireFly to a clock-capable IO pin of the FPGA. FLX-182 would need a revision.

The phase stability of the last hop - FELIX to front-end - depends on the nature of the font-end. If the front-end uses lpGBT ASIC, TCLink is natively supported; if it uses an AMD FPGA, the same considerations for the LTI-FELIX hop apply. No studies performed so far involve Intel FPGA (used by LAr electronics). A survey of front-end technologies has been undertaken by TDAQ management.

5

Hardware Test

5.1 Prototype test plan

This section details the test steps followed by engineers to verify a few prototype samples in the laboratory. The test procedure to be followed to qualify production cards at CERN is presented in Section 5.2.

Power supply Each power rail will be measured before other functionality testing on the board. The testing includes measurement of voltage, current, and ripple. The power-on sequence will be verified to make sure the design meet the requirements from AMD Versal FPGA.

- Power rail short measurement for the INPUT and OUTPUT on every DC/DC
- Bring-up the DC/DC modules one by one without ADM1066
  - Install the voltage configuration resistors
  - Update the compensation resistors
  - Measure the input resistance and make sure it is not a short
  - Double check the remote sense jumpers are correctly set to local monitoring
  - Check the output voltage with scope, and record the ripple
  - Check the switching frequency
  - Check the indication LED
- Connect the 12P0V to two ADM1066
- Configure the ADM1066 with the ADI programmer software
- Power monitoring and sequencer test
- Install the output power jumpers

Card Bring-up

- FT4232 bring up for USB-I2C communication
  - Check the voltage on USB_I2C_VCCIO, should be 3.3V
  - Program the FT4232 with the configuration files provided by FTDI to configure ADBUS to I2C
  - Check I2C operation

  - Configure I2C MUX, and check the sub-I2C buses
- FPGA Bring-up
  - Install heat-sink and fan
  - Measure voltage and ripple of each power rail
  - JTAG configuration via Xilinx platform cable
  - Measure the current consumption of the FPGA

Functionality Test

- Configuration
  - JTAG configuration via the Digilent JTAG module, through USB-C connector on PCIe bracket
  - SD card boot test
  - QSPI boot test
  - Configuration through PCIe with SD card/QSPI
- FPGA I2C test
  - Power monitoring
    - Check INA226 I2C bus, test function of voltage and current monitoring
    - Check TMP435 I2C bus, test function of temperature monitoring
  - On-board clock
    - SI570 for DDR4 memories (200MHz)
    - SI570 for 100 MHz FPGA SYS_CLK100
    - SI570 for 30.33 MHz VERSAL_REF_CLK
    - SI570 for 40.079 MHz SI5345 Input clock
    - SI570 for 40.079MHz ALTI interface clock
    - SI570 for 322.265625MHz 100G refclk for GTY
    - SI511 for 200 MHz FPGA SYS_CLK200
    - SI570 for SI5345
    - SI5345
  - I2C GPIO test
    - I2C configuration test via USB-I2C for TCA6264A
    - I/O GPIO test
- DDR4 bring up
- USB-UART test
- Ethernet port test
- OS operating system bring-up
- Optical communication test via firefly
  - FireFly configuration
  - Loop-back IBERT test
  - External IBERT test
- PCIe Test
  - PCIe clock buffer test

  - PCIe test with loopback card
  - Install the card into a PCIe Gen4 compatible server
  - End-point test via the server
- White Rabbit function test
- Trigger input function test
- Heat-sink fan
  - MAX6643 as fan controller
  - FPGA as fan controller and TACH reading

Performance Test

- Clock measurement
  - GTY reference clock
  - PCIe clock
  - White Rabbit clock
- Optical link performance test
- PCIe performance test

5.2 Self-test web application

A web application has been developed to effectively and efficiently test FELIX cards. A Flask server running on the FELIX PS allows remote PCs to run tests from a remote PC over the network. Test results are visualized in a browser as shown in Figure 5.1. The built-in self test (BIST) requires the card under test to be powered (via the 6-pin connector), to have a network connection to the remote PC (e.g. using the RJ45 socket on the front panel) and, for certain measurements to have a JTAG connection to the remote PC too. The card does not need to be installed in a server, simplifying the test of a large number of cards. The PCIe interface can be tested using a passive loopback adapter.

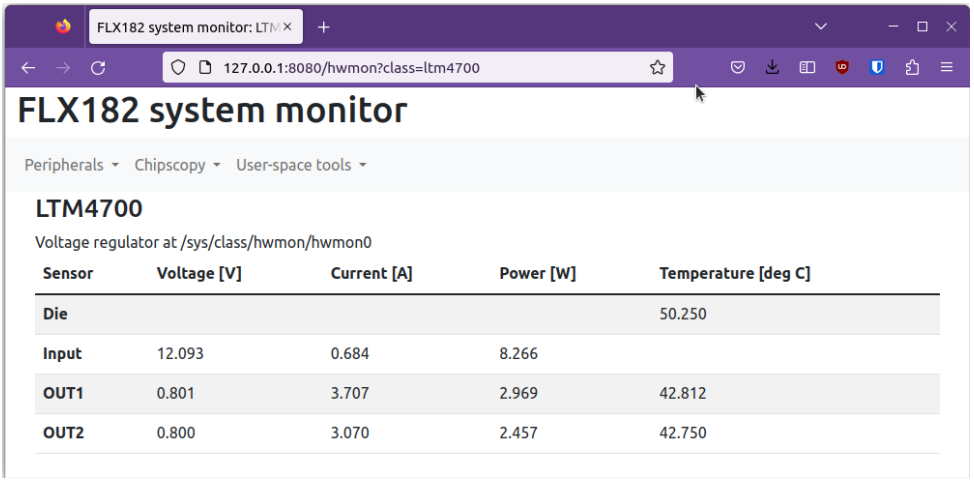


Figure 5.1: Screenshot of BIST from web browser showing monitoring information for the LTM4700 voltage regulator.

The BIST can check the correct status of on-board peripherals: FPGA, LTM4700 power regulator, TMP435 and JC-42.4 temperature sensors, GPIO devices, INA226 power monitor, SI5345 jitter cleaner, ADM1066

power sequencer, and FireFly transceivers. Some test results are shown in Figures 5.2 and 5.3. Through the PS, the Ethernet interface, QSPI flash memory and RAM module (Figure 5.4) can be tested. Finally, with a JTAG connection, IBERT and Open Eye tests can be run. Figure 5.5 shows the open eye test result for 25 Gb/s FireFly modules in physical loopback configuration. Thresholds will be defined for each test portion to determine whether it is passed or failed.

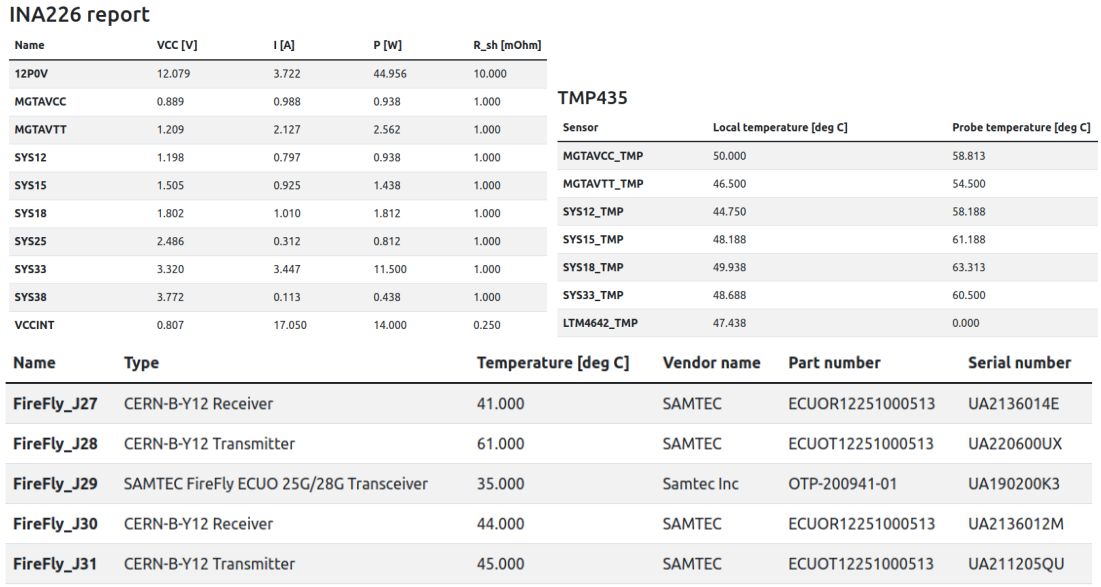


Figure 5.2: Monitoring information from INA226 power rail monitor, TMP435 temperature monitor, SI5345 jitter cleaner test, and installed FireFly modules.

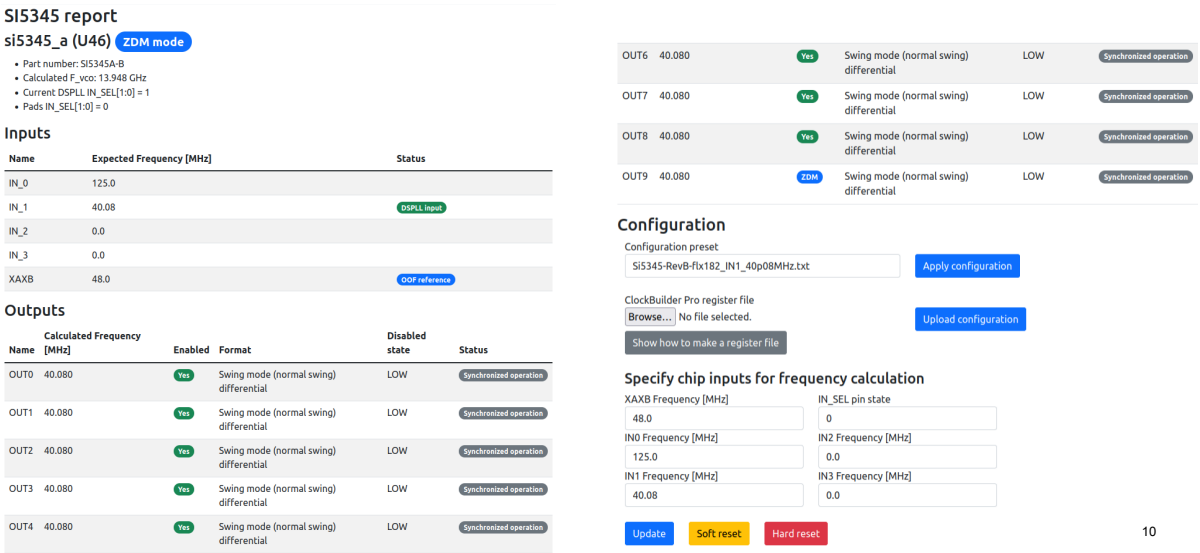


Figure 5.3: Monitoring information from SI5345 jitter cleaner test.

Figure 5.4: Memory test report.

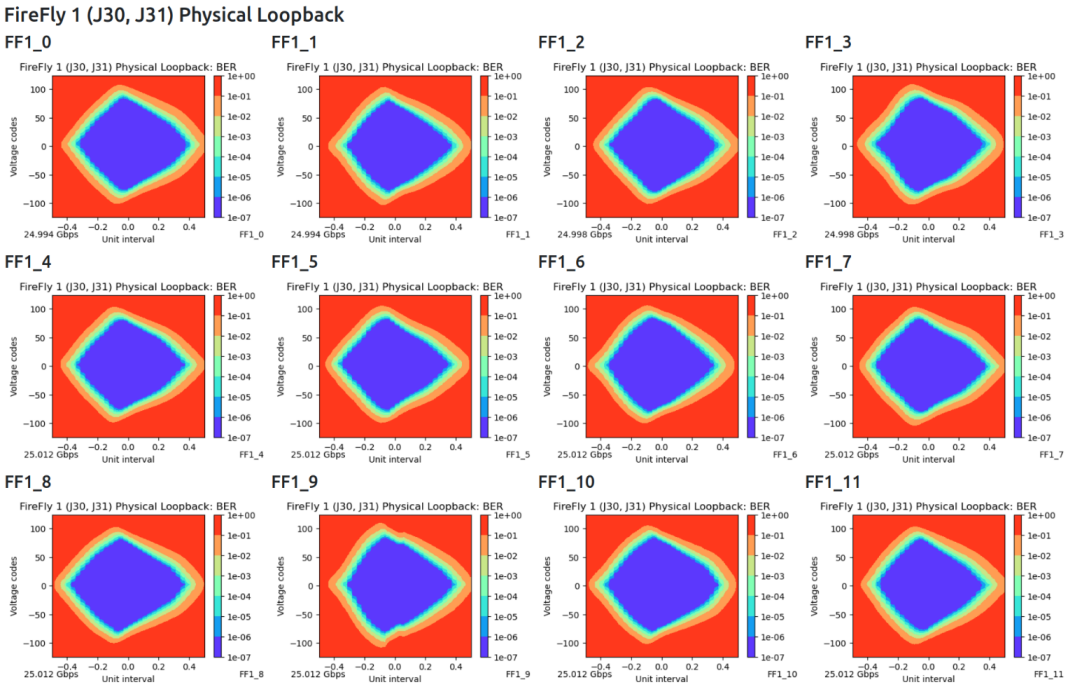


Figure 5.5: Open eye measurement in physical loopback configuration for 25 Gb/s FireFly transceivers.

6 RELIABILITY

6.1 EXPECTED RELIABILITY

The FELIX I/O cards have no industrial comparison, but experience has been gained from the operation of ROBIN and RobinNP cards in Runs 1 and 2 respectively. Taking all failures which have resulted in hardware replacement (including transceiver components) the average incidence rate is less than one per year. Up to date, 10% of the Phase-I FELIX cards, called FLX-712, installed in USA15 were subject to a fan failure. The FLX-712 fan is embedded in the heatsink, sitting on a flat space surrounded by fins. Because of the fan location, the bearing temperature can reach 60 ℃ shortening its lifetime of a factor three (four in terms of L10). The design of FLX-182 and FLX-155 is not subject to the same issue as, in case active cooling is used, the fan sits on top on heatsink fins. As described in Section 3.6, two fans from different manufacturers have been qualified for FLX-182. The preferred fan, Sanyo San Ace 9GA0612H9001, has an expected lifetime (L10) of 40000 hours at 60 ℃, almost double the 22500 hours reported for the FLX-712 fan at the same temperature, and 70000 hours at 40 ℃. The quoted L10 values correspond to a failure of 10% of the installed fans within 5.6 to 9.5 years of continuous operation, approximately covering both Run 4 and 5.

The lifetime of key components used on the FLX-182 design is shown in Table 6.1.

6.2 SPARE PARTS

For all I/O cards and servers a pool of spares, equivalent to 10% of the production system by size, will be procured and maintained. Spares will be deployed both to USA15, to be available for hot and cold swap operations, and also to a separate facility for longer term storage, to be deployed to USA15 to replenish any activated spares. Components subject to aging are FireFly transceivers and the FPGA fan (if present). Both can be readily replaced with spare components without incurring in the risk of damaging the card.

Table 6.1: Lifetime for the major components included on the FLX-182.

Component	Lifetime	
XCVM1802-1MSEVSVA2197 (Xilinx FPGA)	> 20 y @85 ℃	https://www.xilinx.com/support/answers/11768.html
FireFly (4 duplex) (25Gx4 Duplex Optical Module)	> 220 y @40 ℃ > 27.5 y @70 ℃ C	FIT from Samtec FAE
FireFly (14G x12) (14Gx12 Optical Module)	> 71 y @40 ℃ > 23 y @70 ℃	FIT from Samtec FAE
Fan (Sanyo San Ace 60 9GA0612H9001)	MTTF=34 y @60 ℃	Provided by Sanyo
LTM4638/LTM4678/LTM4700 (Power Module)	> 38359 y @55 ℃ > 4794 y @85 ° C	https://www.analog.com/media/en/quality-documentation/r583.pdf
LTM4642 (Power Module)	> 838355 y @55 ℃ > 104794 y @85 ℃	https://www.analog.com/media/en/technical-documentation/reliability-data/r583.pdf
Si5345 (Clock Chip)	> 781 y @85 ℃	https://www.silabs.com/documents/public/miscellaneous/QR-Report.pdf
MT25QU02GCBB8E12-0SIT (QSPI Flash)	> 10 y @65 ℃ > 20 y @55 ℃	https://media-www.micron.com/-/media/client/global/documents/products/technical-note/nor-flash/tn1230_no
ADM1066 (Power Management IC)	> 7150781 y @55 ℃ > 8938 y @85 ℃	https://www.analog.com/en/about-adi/quality-reliability/reliability-data/wafer-fabrication-data.html
DP83867ISRGZT (Ethernet PHY)	> 76940 y @55 ℃ > 9617 y @85 ℃	https://www.ti.com/quality/docs/estimator.tsp#resultstable
TPS51200DRCT (DDR4 Power)	> 1141552 y @55 ℃ > 142694 y @85 ℃	https://www.ti.com/quality/docs/estimator.tsp#resultstable
INA226AIDGSR (Power Monitoring IC)	> 670091 y @55 ℃ > 83761 y @85 ℃	https://www.ti.com/quality/docs/estimator.tsp#resultstable
25SVPF180M (Aluminum Electrolytic Cap.)	> 5000 h @105 ℃ > 36.5 y @45 ℃	https://industrial.panasonic.com/cdbs/www-data/pdf/AAB8000/AAB8000C177.pdf
EEH-ZK1E471P (Aluminum Electrolytic Cap.)	> 4000 h @125 ° C > 29 y @65 ℃	https://industrial.panasonic.com/cdbs/www-data/pdf/AAB8000/AAB8000C177.pdf
EEF-GX0E471R (Tantalum Polymer Cap.)	> 2000 h @105 ° C > 14.5 y @45 ℃	https://industrial.panasonic.com/cdbs/www-data/pdf/RDD0000/ABA0000C1229.pdf

6.3 Quality Assurance

Remark 6.1: *Instructions for this section*

Describe what stress tests will be applied during the development period to validate the reliability of this component. Give a brief outline of any appropriate reliability theory being used. These tests could involve destructive tests. It is not required to complete this section prior to the first specification review but it must be completed prior to the PDR. It is strongly recommended that these plans be reviewed and approved prior to the actual PDR to avoid the possibility of failing the PDR and thus delaying the fabrication or construction of the prototype parts.

6.3.1 Mechanical Reliability Considerations

1. Card should meet the mechanical dimensions as specified, except for additional constraints imposed by the ATLAS experiment and the PCIe specification.
2. Connectors should align to properly mate, pin-by-pin to with each respective interface.
3. Bracket connectors should mate with the specified tolerances for each connector. Mating should be such that no extraneous forces or torque are required.
4. It should be verified that insertion/extraction is properly accomplished within the allowed forces/torque in the specifications.
5. Card components should not intrude into space allocated for the insertion/extraction of a neighboring module.

6.3.2 Electrical Reliability Considerations

1. Card should meet the specifications for impedance, ohmic resistance, and trace length as specified by the layout design sent to the manufacturer. The results of manufacturer's network analyzer test results done prior to delivery will be acceptable.
2. Card ground ohmic contact should be in accordance with specifications to guarantee the flow of undesired currents to the host server ground via the chassis.
3. Correct power sequencing should be verified for each card and should meet the design specifications.
4. All FPGAs should operate within the manufacturer's recommended core temperature to guarantee the required years of operation.
5. All communication lines within the board should be verified and tested for speed and signal integrity.
6. All optical links to and from the board must be verified for transmission accuracy, speed and jitter. As a diagnostic tool, eye diagrams should be obtained for each of the optical TX/RX lines.
7. Correct firmware loading sequence should be observed. Loading should happen without operator's intervention and shall bring the FPGA to its stable operating point within the design allocated time.
8. Each FPGA should be fully functional. Test firmware that will exercise each FPGA and communications between FPGAs will be designed for testing.
9. Cards should not be a source of RF that cause interference to neighboring electronics, or be susceptible to RF interference. This should be verified in pre-production using by fully populating the final server candidate with cards.
10. All non-FPGA components should operate within the specified range as specified by the design.

6.3.3 Operational Reliability Considerations

1. Shake Test: Pre-production cards will be subjected to a shake test to study the reliability of the optical connections. In real operating conditions the card will be placed in an environment with strong air flow that may disrupt optical connections.
2. Vibration Test: A vibration test should be performed on the pre-production board to verify assembly standards.
3. Stress Test: Pre-production cards will be subjected to a stress test. Under this test the board will operate at elevated temperatures for a period of time. The test addresses mis-steps in board assembly, signal integrity, and especially FPGA performance outside of the nominal operating temperatures.
4. Communication errors: Each production card should be tested for communication error rate using the ATLAS agreed upon testing standards.
5. Power failure/recovery: Tests for simulated power failure conditions should be performed. During operations card should be protected from short (~few minutes) power failures, brown outs, power surges and power glitches. In an event that a system failure is observed the board should tolerate any of these conditions without suffering damage.

6.3.4 Environmental Reliability Considerations

Pre-production cards will be tested in the environment of USA15. This test is important to guarantee that there are no environmental issues with the operation of the card. The environmental parameters that may affect the board performance are:

1. Temperature and humidity (including airflow and cooling).
2. Power supply and inrush current in rack.
3. Dust: Optical links are critical for reliable data transmission. One of the most damaging agents for optical links are particulates found in the environment. Past experience has also demonstrated that on-card fans may be degraded by accumulation of particulates if not provided with sufficiently filtered air.
4. Radiation: USA15 is designated as a radiation area, though there are few concerns for long term operations and susceptibility to thermal neutrons.
5. RF environment: pre-production cards will be tested in an environment similar to what will be present in USA15

6.3.5 Additional Tests by Manufacturer

Prototypes and pre-production I/O card samples will be subjected to testing both at the manufacture site and at CERN. A sample of bare PCBs will also be requested to facilitate analysis of the board before component mounting. Low-level tests include:

1. X-rays
2. X-ray fluorescence
3. Thermal cycling
4. PCB cross-sectional analysis (limited cases as this is a destructive test).

At a higher level, tests will also include eye scans and BER tests for links as well as functional and long term performance analysis.

6.4 Quality Control to Validate Reliability Specifications during Production

Each production I/O card will be subjected to testing both at the manufacturer site and at CERN. The types of tests used are the same as those described in Section 6.3, where some (e.g. thermal cycling) will only be performed on a large enough sample of the cards to provide confidence in overall quality. Eye scans, BER tests, functional and performance tests will be performed on all cards.

All procured hardware will be subject to a multi-year manufacturer's warranty covering the operational period.

7

Radiation Tolerance

For ATLAS operations, FELIX hardware will be installed in USA15. The CERN Radiation Protection group of CERN measures the ambient dose equivalent in USA15 to be below 15 µSv/h (threshold for a Radiation Supervised Are). The area has been shielded against thermal neutron radiation to protect both people working in USA15 and the electronics that are installed there. As a consequence, the neutron flux should be reduced significantly. One major concern with the operations of small feature devices near a radiation environment are faults injected by single event effects. The background in USA15 will be mostly thermal neutrons. The main concern is the capture reaction ^{10}B + n, which produces high energy fragments. 20% of the natural boron used for the fabrication of p-type silicon happens to be ^{10}B isotope. The concrete wall thickness and aluminum pipes filled with water provide adequate shielding for personnel and equipment. At present, there are no known cases of observed faults in USA15, especially in FPGAs there installed or in other devices. However, to minimize the sensitivity to this effect manufacturers resort to use depleted boron, or ^{11}B enriched isotope for doping. The FPGAs chosen or FELIX are manufactured using depleted boron. Furthermore, the FPGAs may use internal firmware to detect and correct faults produced by single event effects. The repair mechanism works successfully for low rates of occurrence. In case faults become a serious concern due to unforeseen radiation effects redundant logic can be implemented in the FPGA, where required, along with FPGA memory scrubbing via the JTAG interface.

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Appendix A

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A.1 Glossary

List of Acronyms

ATLAS A Toroidal LHC Apparatus. i

BC Bunch Crossing, The CERN LHC bunch crossing clock frequency is 40.07897 MHz first. 4, 45

CML Current-mode logic. A high-speed digital logic design paradigm that works on the principle of differential current switching. 11

FELIX Front End LInk eXchange. i, 2, 3, 70

FPGA Field Programmable Gate Array. 1

GBT VersatileLink GigaBitTransceiver, a protocol and chip (GBTx) with 4.8Gb/s communication and logical links (E-Links) first. 4

lpGBT low power GigaBitTransceiver, a successor of GBT with 9.6Gb/s Uplink, 2.56Gb/s Downlink and logical links (E-Links) first. 4

LTI Local trigger interface first. 1

MGT Multi-gigabit Transceiver first. 5

PL Programmable logic. 7

PS Processing system: the processor embedded in the chip. 54

SLR Super Logic Region. Trademark name that defined each FPGA tile. 8

TTC Timing, Trigger and Control, a protocol to distribute timing and trigger information first. 1, 45

VTRx+ Versatile Link Plus Transceiver. A radiation-hard optical transceiver developed at CERN. 2