# ATLAS NOTE

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# FLX-712 (BNL-711 V2) Manual

ATLAS FELIX Group

# Contents



# Revision History

| Revision | Date | Author(s) | Description |
|---|---|---|---|
| 0.0 | 12-02-2018 | A. Borga, J. Vermeulen | empty document created |
| 1.0 | 26-02-2018 | K. Chen | complete draft |
| 1.1 | 27-02-2018 | J. Vermeulen | changed to ATLAS template, some updates, added technical details from market survey in appendix |
| 1.11 | 28-02-2018 | J. Vermeulen | added screen shots from A. Borga with output i2c tool |
| 1.12 | 05-03-2018 | W. Panduro Vazquez | editorial pass and reorganisation, adding info on clock and power distribution as well as stackup |
| 1.13 | 06-03-2018 | W. Panduro Vazquez | Minor tweaks to text |
| 1.14 | 06-03-2018 | W. Panduro Vazquez | Implement comments from Andrea, add PRBS testing section. |
| 1.15 | 30-07-2020 | K. Chen | Add new figures for fiber and firmware channel mapping |

| | | | |
|---|---|---|---|
| 1.16 | 18-10-2021 | W. Panduro Vazquez | fix typo in diagram caption |
| 1.17 | 19-10-2021 | W. Panduro Vazquez | update firmware link mapping diagram |

# 1 Overview

The FLX-712 is a 16-lane Gen-3 PCIe card with 48 TX and RX optical links. The on-board FPGA is a Kintex Ultrascale XCKU115FLVF1924-2E. The card hosts a custom form factor Timing Mezzanine Card (TMC), which can be assembled in 3 different configurations. The TMC can interface with: TTC, TTC-PON or white rabbit [1] systems. In the case of ATLAS Phase-I a TTC configuration is used.

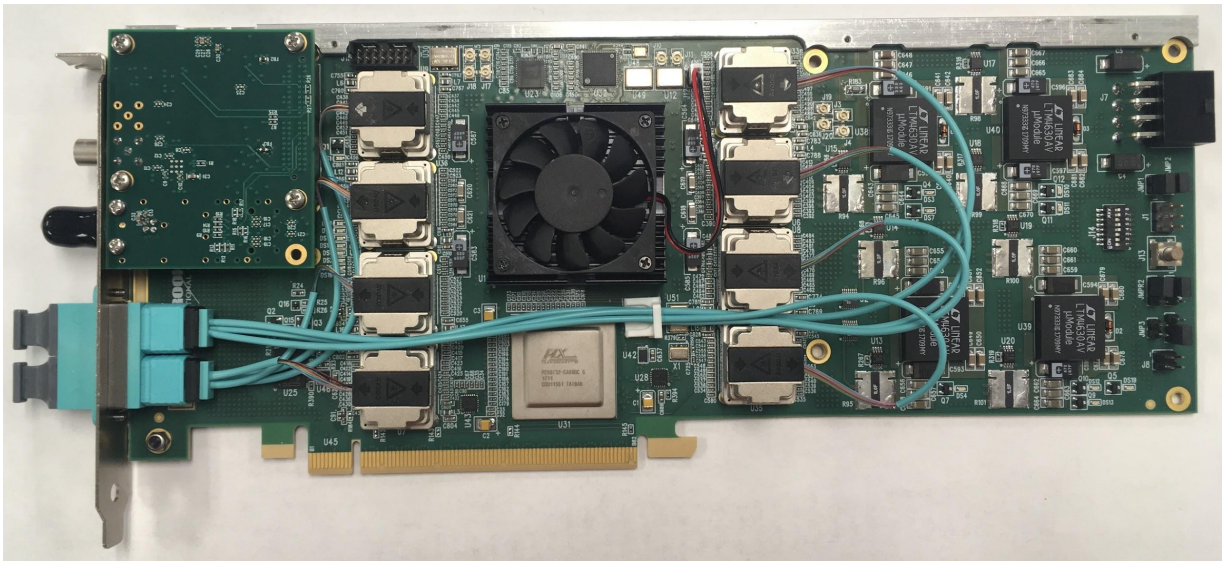

Figure 1: The FLX-712 card with fibres assembled.

# 2 Mechanical Specifications

The FLX-712 is fully compliant with the PCIe 3.0 Standard [2]. Full details are available in Appendix A. A custom made stiffener bar has been produced to strengthen the card. This can be optionally mounted should the host server have enough space for it. The dimensions of the card are:

- Length: 270 mm.
- Width: 110 mm.
- Thickness: 1.58 mm.

# 3 System Architecture

As shown in Figure 2, the card hosts 4 MiniPOD transmitters and 4 MiniPOD receivers. Each MiniPOD has 12 channels. The TTC clock from the ADN2814 is cleaned by an Si5345 or LMK03200. The clean 240 MHz is used as a reference clock for the GTH transceivers. Two of the PCIe hardcore EndPoints within the FPGA are used, with the PEX8732 PCIe switch used to connect them to a 16-lane slot. The full FPGA Pinout is available in the official FPGA documentation [3]. An on-board 2 Gb FLASH memory can store 4 different firmware bit files. An on-board microcontroller (which the host can communicate with either via SMBus or through the FPGA and PCIe interface) can be used to select one of the four FLASH memory partitions and trigger FPGA programming from the image stored in the selected partition. The microcontroller-based model is inspired by that which was used for the ALICE C-RORC [4]. On power-up the FPGA is programmed with the image from the partition that is selected by two jumpers. More information on this is available in Section 4. A direct JTAG connection for FPGA programming is also available. The FLASH memory can be loaded with bit files via both the PCIe interface and JTAG.

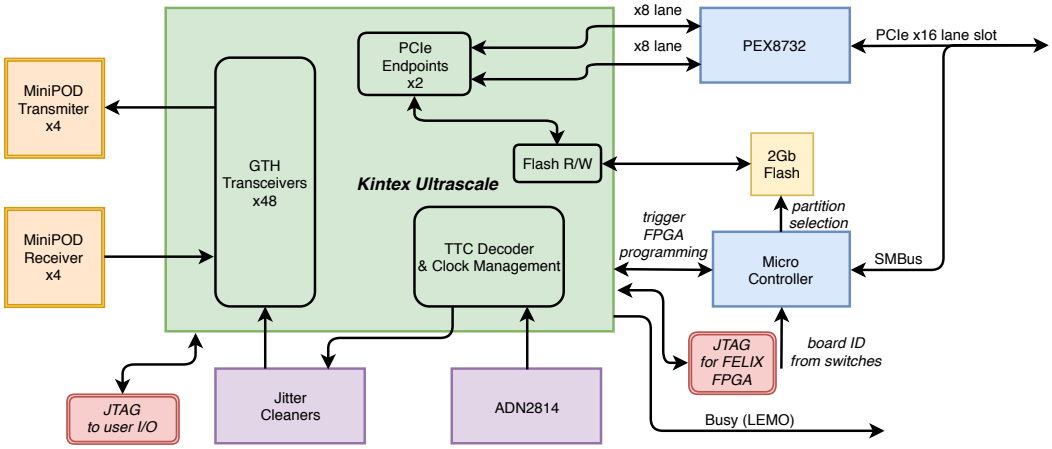


Figure 2: Functions of the FLX-712.

## 3.1 FPGA Bank Layout

As shown in Figure 3, the FPGA has two Super Logic Regions (SLRs). To balance resource usage and minimise the number of traces crossing the boundary each SLR has one 8-lane PCIe endpoint. These are connected to bank 226/227 and 229/230. A transceiver in bank 231 can be connected to either a MiniPOD or to an SFP on a mezzanine card equipped with an SFP by changing the capacitor assembly. The banks depicted as white boxes in Figure 3 exist in the XCKU115FLVF1924-2E FPGA used on the card, but are not available in a XCKU085-FLVF1924 FPGA. The rest of the FPGAs are pin-to-pin compatible. The 085 could be used as a more cost effective alternative to the 115 if needed. For the 24-ch GBT firmware flavour banks 126-128 and 131-133 will be used.

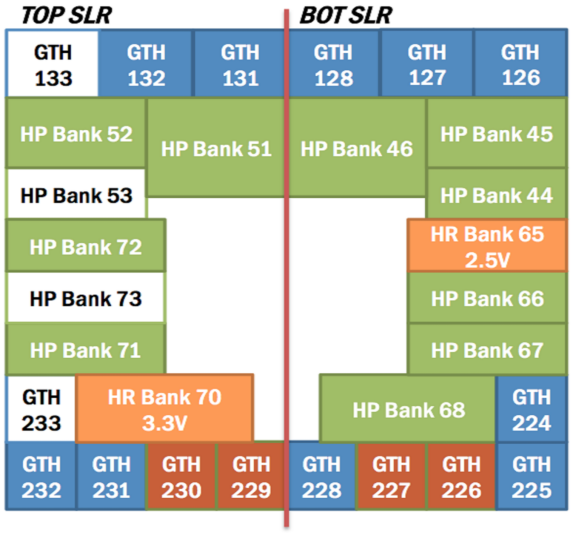


Figure 3: FPGA bank usage. GTH banks provide high speed serialisers (4 per bank), HP (High Performance, max 1.8V signalling) and HR (High Range, max. 2.5V or 3.3V signalling) banks connect to user I/O pins.

## 3.2 Power Supply

A single +12V power line is supplied to the card via an on-board 8-pin connector as in Figure 4.

| 6-pin power connector (75 W)[16] | | 8-pin power connector (150 W)[17][18][19] | |
|---|---|---|---|
| Pin | Description | Pin | Description |
| 1 | +12 V | 1 | +12 V |
| 2 | Not connected (usually +12 V as well) | 2 | +12 V |
| 3 | +12 V | 3 | +12 V |
| | | 4 | Sense1 (8-pin connected[a]) |
| 4 | Ground | 5 | Ground |
| 5 | Sense | 6 | Sense0 (6-pin or 8-pin connected) |
| 6 | Ground | 7 | Ground |
| | | 8 | Ground |


6 pin power connector pin map


8 pin power connector pin map

a. ^ When a 6-pin connector is plugged into an 8-pin receptacle the card is notified by a missing *Sense1* that it may only use up to 75 W.

Figure 4: Pin mapping of the PCIe power connector.

As per the PCIe specification, there are three kinds of PCIe power cables which can be connected to the on-board 8-pin connector. These are shown in Figure 5. As well as the 8 pin option, sufficient power can also be provided through a cable with a 6 pin connector, or with a 6+2 pin connector (of which the 6-pin part is used). The FLX-712 uses 4 dual 18A regulators (LTM4630A). In order to meet the power sequence requirements of Xilinx FPGAs they are enabled in 3 stages, as shown in Figure 6. The sequencing is arranged by using the power-good signal from a given stage to trigger the power-enable of the next stage. Full details of the AC and DC power characteristics of the FPGA can be found in the official documentation [5].


(a) 6 pin. (b) 8 pin. (c) 6+2 pin.

Figure 5: Pictures of PCIe Power Cables


Figure 6: FLX-712 Power Distribution Staging.

## 3.3 Timing System

The ability to host different mezzanine cards implementing timing interfaces means three systems are supported:

- ATLAS TTC (Timing, Trigger and Control), with mezzanine shown in Figure 1. Main components on the card are: TC ORx, ADN2814 (clock and data recovery chip) and LEMO output for BUSY.
- TTC-PON or any clock system using SFP.
- White Rabbit configuration.

The timing mezzanine is supported by two different kinds of brackets: one is compatible with the TTC version, the other for the other two systems. TTC is the standard FELIX configuration for ATLAS Phase-I. The mezzanines themselves can be seen in Figure 7.

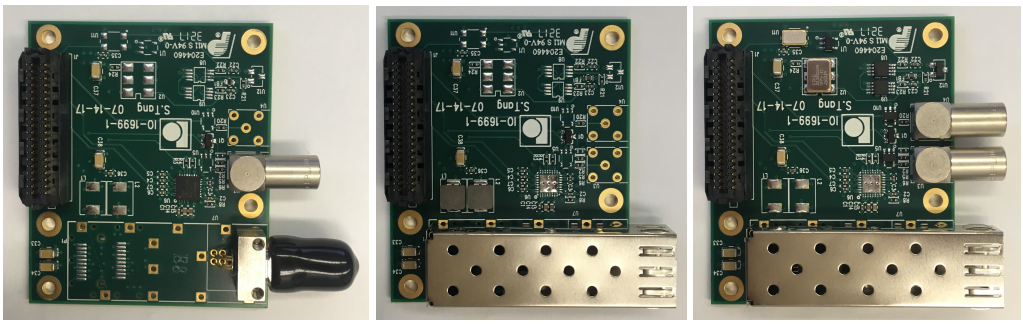

Figure 7: FLX-712 Mezzanines with interfaces for: (left) TTC, (centre) TTC-PON and (right) White Rabbit.

## 3.4 Clock Distribution

The FLX-712 has two on-board clock jitter cleaners: the Si5345 (used by FELIX); and the LMK03200 (used as a backup). The clock distribution is shown in Figure 8. Both jitter cleaners are configurable over I2C (see next section) with custom applications available in the FELIX software release. The Si5345 takes two inputs FPGA and a third from an SMP connector (optional). A fourth input is fed by the last output, to guarantee 0-delay. For FPGA banks 126-128 and 131-133 each quad can use its own clock (and those of its neighbours) as reference. For banks 224-228 and 229-233 each quad can use its own clock as reference, as well as those of its neighbours and neighbour's-neighbours. With the exception of banks 224/225/228 all other quads can use two outputs from the Si5345. Banks 224/225/228 can instead use one output from the Si5345 and one output from the LMK03200. For more information please consult the official FPGA documentation for clocking [6] and GTH transceivers [7].

## 3.5 I2C Buses

The purpose of the FLX-712's I2C facility is to provide environmental monitoring of the physical health of card and to make it possible to configure on-board programmable clock sources.

The FLX-712 has three on-board I2C switches. As shown in Figure 9, one is connected to the FPGA. This switch can be controlled with the flx-i2c tool. A second switch is connected to the SMBus interface in

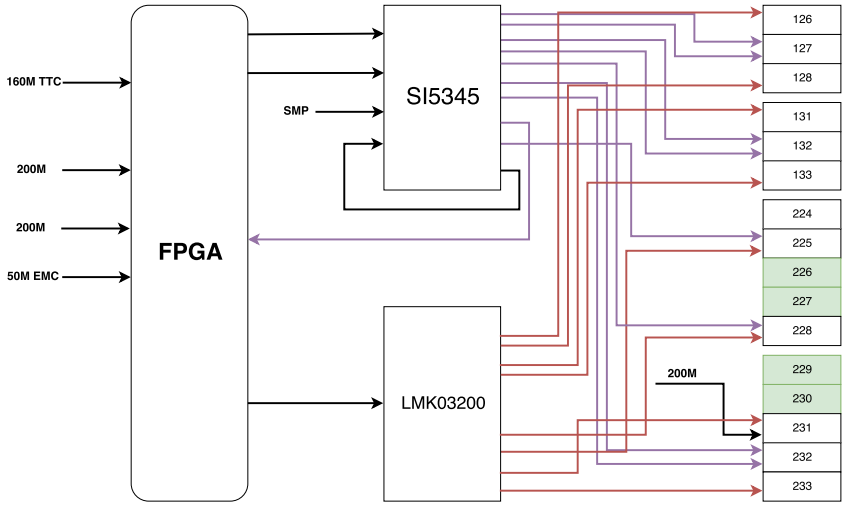


Figure 8: FLX-712 Clock Distribution Scheme.

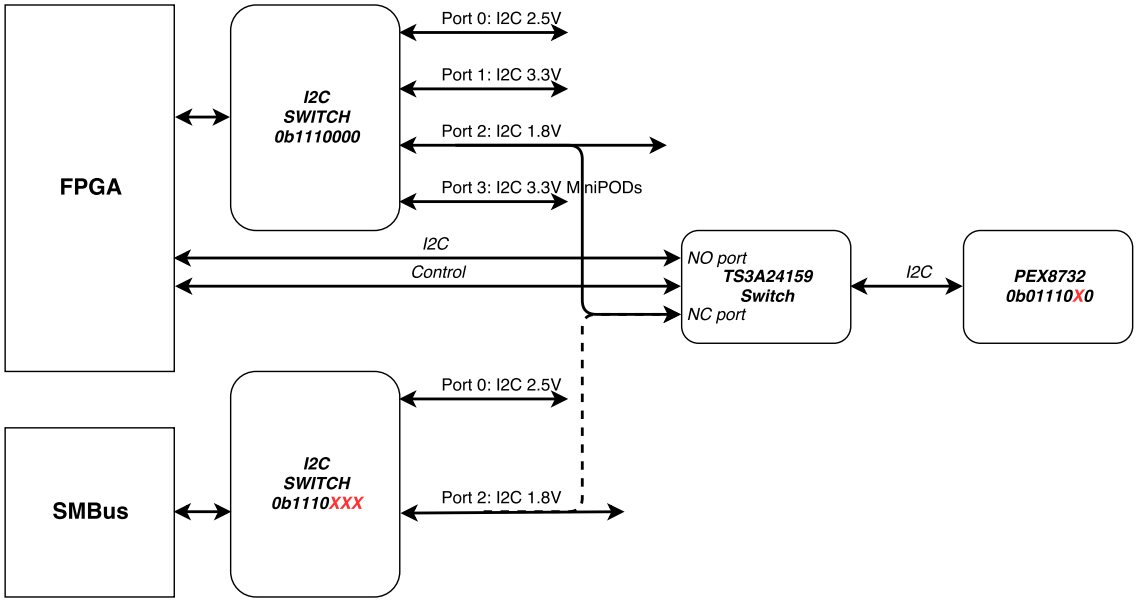


Figure 9: FLX-712 I2C buses. The dashed line indicates an optional connection (requires placement of a resistor). Switch connected to FPGA is U50. Switch connected to SMBus is U10.

the PCIe slot. The slaves are listed in Table 1, with U50 referring to the switch connected to the FPGA. The third switch is connected both to the first switch and to the FPGA and is used for control of the PEX PCIe switch from either the SMBus or the FPGA. For examples of available monitoring information see Figures 11 and 12. This temperature information can be used to check card status, especially for FPGA and PEX switch. When all the 48 optical links are used (for example LTDB firmware mode), the fan speed in the server can be increased by using **ipmitool**.

| Components | I2C address | connected to |
|---|---|---|
| PCA9546: U50 | 1110000 | FPGA |
| RX MiniPODs | 01100XX | U50: port 3 |
| TX MiniPODs | 01011XX | U50: port 3 |
| Si53154 | 1101011 | U50: port 1 |
| ADN2814 | 1000000 | U50: port 1 |
| LTC2991: U2 | 1001000 | U50: port 1 |
| LTC2991: U3 | 1001001 | U50: port 1 |
| Si5345 | 11010XX | U50: port 2 |
| PCA9546: U10 | 1110XXX | SMBus |
| ATMEGA324A | XXXXXXX | SMBus: port 0 and FPGA |
| PEX8732 | 01110X0 | FPGA port 1 and U50 port 2 |

Table 1: I2C slaves. PCA9546: I2C switch connecting to SMBus, LTC2991: voltage, current and board temperature monitor chip, Si53154: PCIe clock fanout, ATMEGA234A: microcontroller.

# 4 FPGA Configuration

FPGA firmware can be programmed over JTAG or from the on-board FLASH memory (see Figure 10, it is BP30 flash for some early prototypes, and MT28FW02GB for production cards). There are two ways to load the memory firmware images into the memory: via JTAG or dedicated FPGA firmware. By default the FLASH memory is controlled by JTAG. The FELIX software can switch control to the FPGA and update the FLASH memory via registers in PCIe BAR2. The FLASH memory can store four bit files, with partition selection able to be controlled by firmware, microcontroller or jumpers. The firmware has the highest priority, while the jumpers (JMPR1 and JMPR2) have the lowest priority.

If the microcontroller is used for selection the uC_FLASH_A25 and uC_FLASH_A26 (see Table 2) being set to value '1' will set the A25 and A26 memory address lines to value '0' respectively. If Jumpers are used for selection the same rule holds. But software **fflash** mapping is based on microcontroller. So the first partition is actually A25=1, A26=1, or JMPR1.2 shoud be connected to JMPR1.1 and JMPR2.2 to JMPR2.1. The second partition is A26=1, A25=0, or JMPR1.2 shoud be connected to JMPR1.3 and JMPR2.2 to JMPR2.1. The third partition is A26=0, A25=1, or JMPR1.2 shoud be connected to JMPR1.1 and JMPR2.2 to JMPR2.3. The 4th FLASH partition is A25=0, A26=0, or JMPR1.2 shoud be connected to JMPR1.3 and JMPR2.2 to JMPR2.3.

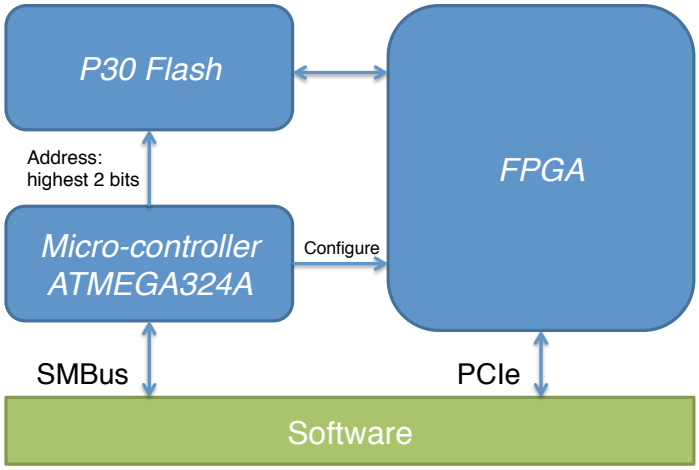


Figure 10: The FLASH memory and microcontroller used for firmware version control.

| | |
|---|---|
| JMPR1.1 | GND, closeer to PCIe power connector |
| JMPR1.2 | uC_FLASH_A25 |
| JMPR1.3 | SYS25 (2.5 V) |
| JMPR2.1 | GND, closeer to PCIe power connector |
| JMPR2.2 | uC_FLASH_A26 |
| JMPR2.3 | SYS25 (2.5 V) |

Table 2: Jumpers for FLASH partition selection. JMPR1.2 can be connected either to JMPR1.1 or JMPR1.3 to set memory address line A25 to 1 or 0 respectively. JMPR2.2 can be connected either to JMPR2.1 or JMPR2.3 to set memory address line A26 to 1 or 0 respectively.

## 4.1 Microcontroller Usage

The purpose of the on-board microcontroller (ATMEGA324A) is to control the remote (re)configuration of the FPGA and its FLASH via the SMBus. The I2C slave available in the microcontroller firmware can be communicated with from the host PC Operating System's standard software. The controller can send an initialization signal to the FLASH and can select a FLASH partition. It also makes it possible to trigger FPGA programming and monitor programming status. As there are several pins connected to FPGA, firmware can also be implemented to support similar operations to flx-i2c[1]. The microcontroller comes pre-programmed with a FELIX 'factory image' and should be ready to use.

```
Parameters of the First LTC2991
|Parameter                        | Value     | Unit|
|================================ | ========= | ====|
|VCCINT current                   |   7.20928 |    A|
|VCCINT voltage                   |   0.95460 |    V|
|MGTAVCC current                  |   2.97477 |    A|
|MGTAVCC voltage                  |   2.97477 |    V|
|FPGA internal diode temperature  |  51.06250 |    C|
|MGTAVTTC voltage                 |   0.07599 |    V|
|MGTVCCAUX voltage                |   7.20928 |    V|
|LTC2991_1 internal temperature   |  32.25000 |    C|
|VCC                              |   3.30842 |    V|

Parameters of the Second LTC2991
|Parameter                          | Value     | Unit|
|================================== | ========= | ====|
|PEX0P9V current                    |   5.59288 |    A|
|PEX0P9V voltage                    |   0.93263 |    V|
|SYS18 current                      |   1.13831 |    A|
|SYS18 voltage                      |   1.79995 |    V|
|SYS12 voltage                      |   0.00000 |    V|
|SYS25 voltage                      |   2.48691 |    V|
|PEX8732 internal diode temperature |  44.18750 |    C|
|LTC2991_2 internal temperature     |  30.93750 |    C|
|VCC                                |   3.31025 |    V|
```

Figure 11: Example of the information available from the LTC2991 chips (from software).

```
MiniPODs
========
Note: 814=receiver, 824=transmitter

               | 1st 814 | 2nd 814 | 3rd 814 | 4th 814 | 1st 824 | 2nd 824 | 3rd 824 | 4th 824 |
               |=========|=========|=========|=========|=========|=========|=========|=========|
Temperature [C]|    43.9 |    38.9 |    39.3 |    41.4 |    44.4 |    36.6 |    38.4 |    39.1 |
3.3 VCC     [V]|    3.26 |    3.26 |    3.26 |    3.28 |    3.29 |    3.29 |    3.29 |    3.28 |
2.5 VCC     [V]|    2.42 |    2.42 |    2.44 |    2.45 |    2.38 |    2.43 |    2.44 |    2.42 |

LOS latched of channel: | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
                        |===|===|===|===|===|===|===|===|===|===|====|====|
                1st 814 | N | N | N | N | N | N | N | N | Y | Y |  Y |  Y |
                2nd 814 | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y |  Y |  Y |
                3rd 814 | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y |  Y |  Y |
                4th 814 | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y |  Y |  Y |
                1st 824 | N | N | N | N | N | N | N | N | Y | Y |  Y |  Y |
                2nd 824 | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y |  Y |  Y |
                3rd 824 | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y |  Y |  Y |
                4th 824 | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y |  Y |  Y |

                |        1st 814 |        2nd 814 |        3rd 814 |        4th 814 |        1st 824 |        2nd 824 |        3rd 824 |        4th 824 |
                |================|================|================|================|================|================|================|================|
Name            | AVAGO          | AVAGO          | AVAGO          | AVAGO          | AVAGO          | AVAGO          | AVAGO          | AVAGO          |
OUI             | 0x00 0x17 0x6a | 0x00 0x17 0x6a | 0x00 0x17 0x6a | 0x00 0x17 0x6a | 0x00 0x17 0x6a | 0x00 0x17 0x6a | 0x00 0x17 0x6a | 0x00 0x17 0x6a |
Part number     | AFBR-814FN1Z   | AFBR-814FN1Z   | AFBR-814FN1Z   | AFBR-814FN1Z   | AFBR-824FN1Z   | AFBR-824FN1Z   | AFBR-824FN1Z   | AFBR-824FN1Z   |
Revision number | 32 32          | 32 32          | 32 32          | 32 32          | 32 32          | 32 32          | 32 32          | 32 32          |
Serial number   | A171950C3      | A171950BC      | A171950A2      | A171950AE      | A1719409B      | A1719408C      | A17194091      | A1719407V      |
Date code       | 2017051        | 2017051        | 2017051        | 2017051        | 2017051        | 2017051        | 2017051        | 2017051        |
```

Figure 12: Example of the information available from the MiniPODs (from software).

In order to update the microcontroller firmware the following are required: an AVR Dragon tool, 6-pin cables and Atmel Studio 7 for software control. The programming files can be obtained from gitlab:

[1] For production, two pins will be connected to the FPGA I2C bus in Figure 9, then flx-i2c will be used both to select flash partitions and trigger FPGA programming

https://gitlab.cern.ch/atlas-tdaq-felix/felix-fpga-flash

The steps to update the microcontroller are:

- Connect the 6-pin cable from the AVR dragon board to J1 of the FLX-712.
- Connect the AVR dragon board via USB to a Windows PC with Atmel Studio 7.
- Open Studio 7, click 'Tools', then select 'Device Programming'.
- Set the 'Tool' option to 'AVR Dragon'; 'Device' to 'ATmega324A'; and 'Interface' to ISP. Read the device signature and verify that it is 0x1E9515. Check that the Target Voltage is 2.5V.
- Go to 'Memories' in 'Flash (32 KB)' and select the .elf file to be used. Check "Erase device before programming" and "Verify Flash after programming", then click 'Program'. Wait for the results.

### 4.2 Software Control of FLASH & FPGA Programming

The board will be provided with four reference firmware revisions, one in each FLASH partition. Each revision makes it possible to write to the other three partitions. To manage the FLASH update, and program the FPGA with the resulting bit file, several pieces of software must be used. Firstly, the SMBus interface (software supplied by OS) controls the microcontroller, making it possible to select FLASH partitions and trigger reprogramming of the FPGA from a partition. Second, as part of the FELIX software release, the 'fflash' tool is provided. This interfaces with and controls the SMBus OS software, and manages the programming of the FLASH itself. Finally, PCIe hotplug (software supplied by OS) makes it possible to re-initialise the PCIe Bus and pick up the new FPGA configuration. With all of these features in place it should be possible to reprogram the FLASH and FPGA without the need for any reboots of the host system. For more information on please consult the FELIX user manual [8].

## 5 Jumpers & Switches

All on-board Jumpers and switches are located close to the power connector. One 8-pin switch is used for I2C addresses, as shown in Table 3. For JMPR1 and JMPR2 see Table 2.

| bits | usage |
|---|---|
| 2-0 | PCA9546: U10 I2C address bit 2-0 |
| 5-3 | connected to ATMEGA324A, can be used as address |
| 6 | connected to PEX8732, sets PEX address bit 1 |
| 7 | connected to FPGA |

Table 3: Switch for address selection.

Other available jumpers and their usage are listed below.

- J1: For microcontroller configuration with 6-pin ISP programmer (see Section 4.1)

| | |
|---|---|
| 1 | MISO |
| 2 | VTG-SYS25 |
| 3 | SCK |
| 4 | MOSI |
| 5 | RSTn |
| 6 | GND |

- J2: PRSNT selection: 2&3 are connected. PRSNT is the "Present" finger in the PCIe connector to inform the PC that the card is present. PRSNT_FPGA is an output pin of the FPGA and PRNST1 is another finger of the PCIe connector that is controlled by the PC.

| | |
|---|---|
| 1 | PRSNT_FPGA |
| 2 | PRSNT |
| 3 | PRSNT1 |

- J8: backup I2C/SMB connector.

| | |
|---|---|
| 1 | SYS33 (3.3V) |
| 2 | PCIE_SCL |
| 3 | GND |
| 4 | PCIE_SDA |

- JMP1: connect FPGA_PROG_B to the uC_FPGA_PROG_B (PC5). Connected by default.

| | |
|---|---|
| 1 | uC_FPGA_PROG_B |
| 2 | FPGA_PROG_B |

- JMP2: connect FPGA_INIT_B to the uC_FPGA_INIT_B (PD2). Connected by default.

| | |
|---|---|
| 1 | uC_FPGA_INIT_B |
| 2 | FPGA_INIT_B |

- JMP3: WAKE_N from PCIe to FPGA for wake-up functionality. Not connected by default.

| | |
|---|---|
| 1 | PCIE_WAKE_N |
| 2 | PCIE_WAKE_N_FPGA |

- J13: button to reset microcontroller.

# 6 Fibre Mapping

Every FLX-712 comes with PRIZM patches pre-installed, connecting the MTP inputs to the MiniPODs. These patches are custom made for the card and mean that the users should only need to connect to their data source to the MTP cable. No internal cabling work on the FLX-712 is required. The Fibre mapping and pin assignment for channels in each MiniPODs are shown described in this section. Two configurations are shown here: 48 channel and 24 channel. For 48 channel version, there are 24-TX and 24-RX in fibre connected to each MTP coupler. For 24 channel version, the channel number is 12 for each MTP coupler. For current MTP coupler, the Key are at different position for the two sides, details can be found by comparing Figure 14 and 15.

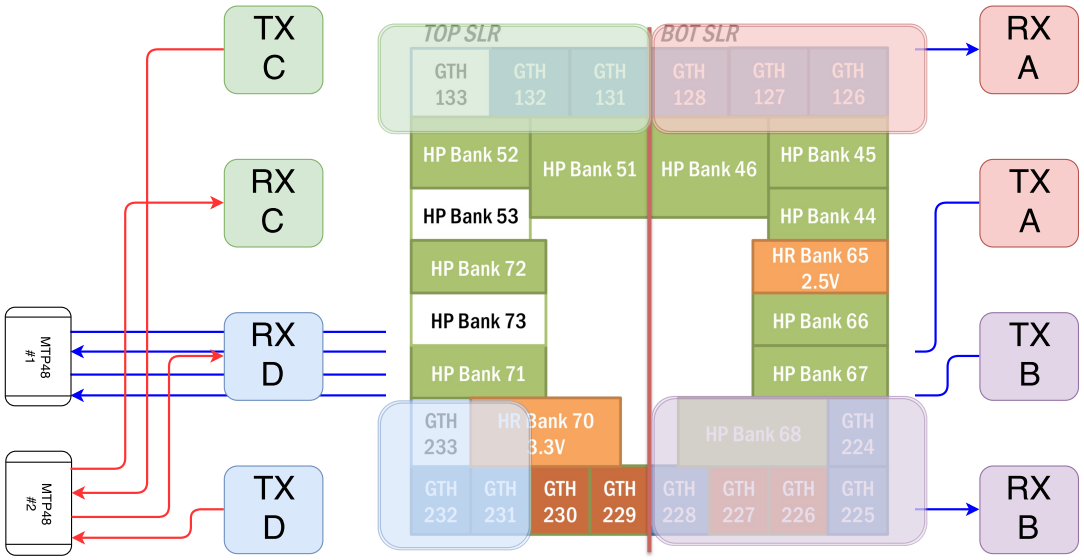


Figure 13: 48-ch configuration.

Key

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| RXA12 | RXA11 | RXA10 | RXA9 | RXA8 | RXA7 | RXA6 | RXA5 | RXA4 | RXA3 | RXA2 | RXA1 |
| TXA12 | TXA11 | TXA10 | TXA9 | TXA8 | TXA7 | TXA6 | TXA5 | TXA4 | TXA3 | TXA2 | TXA1 |
| RXB12 | RXB11 | RXB10 | RXB9 | RXB8 | RXB7 | RXB6 | RXB5 | RXB4 | RXB3 | RXB2 | RXB1 |
| TXB12 | TXB11 | TXB10 | TXB9 | TXB8 | TXB7 | TXB6 | TXB5 | TXB4 | TXB3 | TXB2 | TXB1 |

Key

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| RXC12 | RXC11 | RXC10 | RXC9 | RXC8 | RXC7 | RXC6 | RXC5 | RXC4 | RXC3 | RXC2 | RXC1 |
| TXC12 | TXC11 | TXC10 | TXC9 | TXC8 | TXC7 | TXC6 | TXC5 | TXC4 | TXC3 | TXC2 | TXC1 |
| RXD12 | RXD11 | RXD10 | RXD9 | RXD8 | RXD7 | RXD6 | RXD5 | RXD4 | RXD3 | RXD2 | RXD1 |
| TXD12 | TXD11 | TXD10 | TXD9 | TXD8 | TXD7 | TXD6 | TXD5 | TXD4 | TXD3 | TXD2 | TXD1 |

Figure 14: 48-ch fibre mapping.

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| RXA12 | RXA11 | RXA10 | RXA9 | RXA8 | RXA7 | RXA6 | RXA5 | RXA4 | RXA3 | RXA2 | RXA1 |
| TXA12 | TXA11 | TXA10 | TXA9 | TXA8 | TXA7 | TXA6 | TXA5 | TXA4 | TXA3 | TXA2 | TXA1 |
| RXB12 | RXB11 | RXB10 | RXB9 | RXB8 | RXB7 | RXB6 | RXB5 | RXB4 | RXB3 | RXB2 | RXB1 |
| TXB12 | TXB11 | TXB10 | TXB9 | TXB8 | TXB7 | TXB6 | TXB5 | TXB4 | TXB3 | TXB2 | TXB1 |

Key

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| RXC12 | RXC11 | RXC10 | RXC9 | RXC8 | RXC7 | RXC6 | RXC5 | RXC4 | RXC3 | RXC2 | RXC1 |
| TXC12 | TXC11 | TXC10 | TXC9 | TXC8 | TXC7 | TXC6 | TXC5 | TXC4 | TXC3 | TXC2 | TXC1 |
| RXD12 | RXD11 | RXD10 | RXD9 | RXD8 | RXD7 | RXD6 | RXD5 | RXD4 | RXD3 | RXD2 | RXD1 |
| TXD12 | TXD11 | TXD10 | TXD9 | TXD8 | TXD7 | TXD6 | TXD5 | TXD4 | TXD3 | TXD2 | TXD1 |

Key

Figure 15: 48-ch fibre mapping looking from MTP coupler.

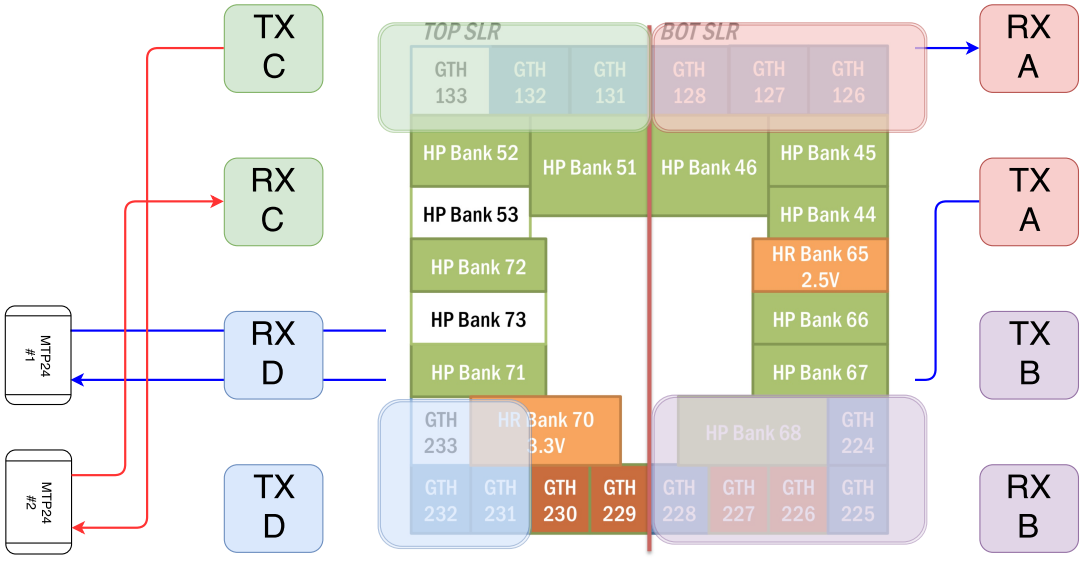


Figure 16: 24-ch configuration.

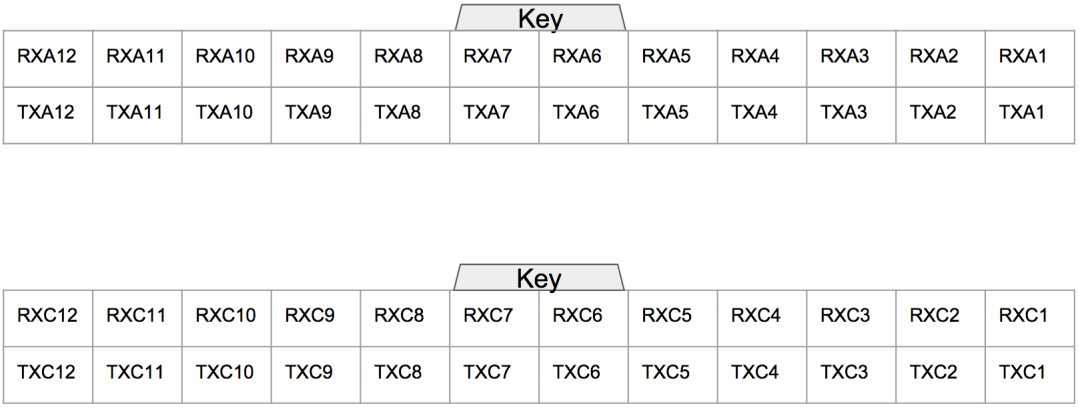


Figure 17: 24-ch fibre mapping.

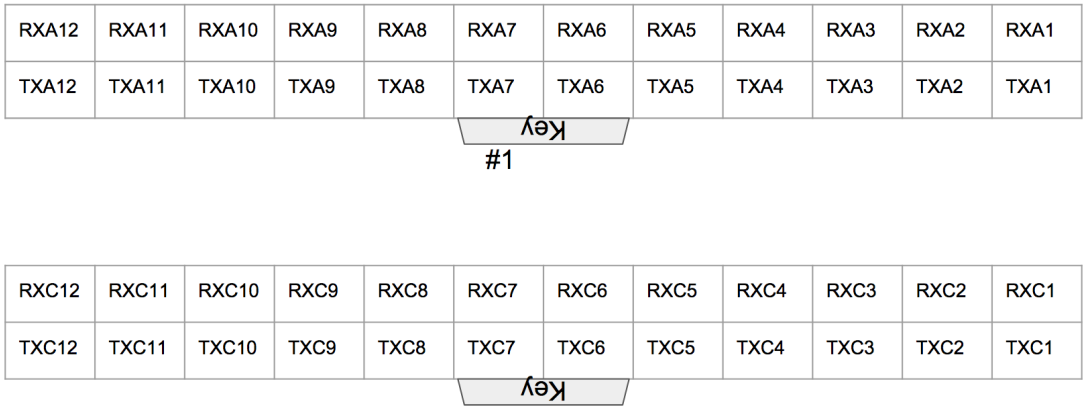


Figure 18: The 24-ch fibre mapping looking from MTP coupler.

| Group A | RX_P | Group B | RX_P | Group C | RX_P | Group D | RX_P |
|---|---|---|---|---|---|---|---|
| 1 | AC43 | 1 | AG2 | 1 | C43 | 1 | J2 |
| 2 | AG43 | 2 | AF4 | 2 | E43 | 2 | H4 |
| 3 | AE43 | 3 | AC2 | 3 | G43 | 3 | G2 |
| 4 | AF41 | 4 | AE2 | 4 | J43 | 4 | F4 |
| 5 | AH41 | 5 | BA10 | 5 | L43 | 5 | C2 |
| 6 | AJ43 | 6 | BC10 | 6 | N43 | 6 | E2 |
| 7 | AN43 | 7 | AY8 | 7 | R43 | 7 | B4 |
| 8 | AL43 | 8 | BB12 | 8 | U43 | 8 | D4 |
| 9 | AU43 | 9 | BB4 | 9 | W43 | 9 | C10 |
| 10 | AR43 | 10 | BD4 | 10 | V41 | 10 | A6 |
| 11 | BA43 | 11 | BA2 | 11 | AB41 | 11 | B12 |
| 12 | AW43 | 12 | BC6 | 12 | AA43 | 12 | E10 |

Figure 19: FPGA GTH Pin mapping for the MiniPODs.

# 7 PRBS Testing

Link speed testing has been performed on 17 currently latest version FLX-712 prototypes. The average open area results for IBERT in 9.6 Gp/s is shown in Table 4. The average bit error rate (BER) was lower than $1 \times 10^{-15}$. Some indicative eye diagrams are presented in Figures 20. The 12.8 Gb/s test is also carried out on a few cards, the open area is around 6500.

| Link Speed | PLL type | Average Open Area |
|---|---|---|
| 9.6 Gb/s | QPLL1 | 9049 |

Table 4: IBERT Test Results for FLX-712 prototypes: 9.6 Gb/s.

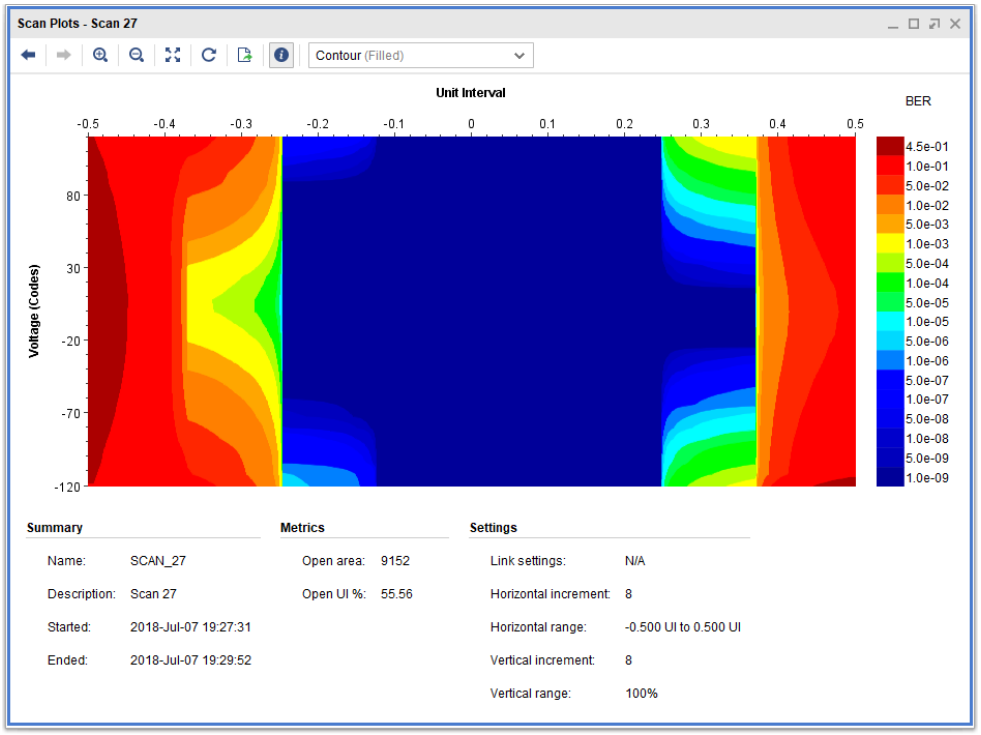


Figure 20: Eye diagram for link speed test at 9.6 Gb/s. Open area is 9152.

# Appendix

## A PCB details

Fabrication and stackup information for the FLX-712 are shown in Figure 21. The PCB is 16 layers thick. There is one blind via from the top layer to layer 7 for high speed traces between the FPGA and the MiniPODs. PCB fabrication involves two laminations. The key parameters for PCB production are:

- Overall PCB dimensions: 273.94 x 111.15 mm PCI Express card according to PCI Express Card Electromechanical Specification Revision 3.0;

- 16 layer Megtron-6 material with a maximum overall thickness of (1.57 ± 0.13) mm
- 0.5 & 1 oz. copper
- 69/81/89 um core & prepreg
- 0.08 mm min. trace width and clearance
- Full & blind vias, 2 drill groups (1-16 for through hole vias, 1-7 for blind vias)

# B Acceptance and acceptance tests at the production site

All cards produced shall be tested before shipping to CERN. The contractor shall perform these tests:

- Electrical test of the PCB before assembly according to IPC-D-356 (netlist)
- Visual inspection of the assembled board
- Radiography of all modules in order to check the quality of the assembly
- Thermal cycle: Each module has to be subjected to two thermal cycles according to the IPC9701A standard
- Power-on tests of the assembled board following a checklist provided by CERN
- Installation of the card into a PC and execution of a test routine provided by CERN. This includes the programming of the FPGA with firmware provided by CERN and the installation of MiniPOD transceivers and fibre assemblies

A server PC as well as any components of the test bench that are specific to the supplies will be provided free of charge by CERN. These will remain the property of CERN for the duration of the contract, in accordance with clause 15 of the General Conditions of CERN Contracts. The contractor will use these to perform a custom test specified by CERN. CERN will also provide software for the execution of functional tests.

# C Fiber mapping and firmware channel mapping

The mapping between the Xilinx FPGA transceiver pins to the female MTP fiber connector inserted into MTP adapter are shown in Figure 22 and 23. The first one in each figure is for the adapter close to the PCIe connector and mapped to minipods ont the right side of FPGA. The second one is for the adapter close to TTC connector, and mapped to minipods on the left side of FPGA. As shown in Figure 22, BB8 and BC6 are one pin of the differential GTH TX and GTH RX pins, belong to a same GTH transceiver. This is the same for all other GTH pairs, for example AY4/BA2 and so on.

For different firmware modes, the firmware channels are mapped to different GTH transceiver. The detailed mapping can be found in Figure 24, for 8, 16, 24 and 48 cases.

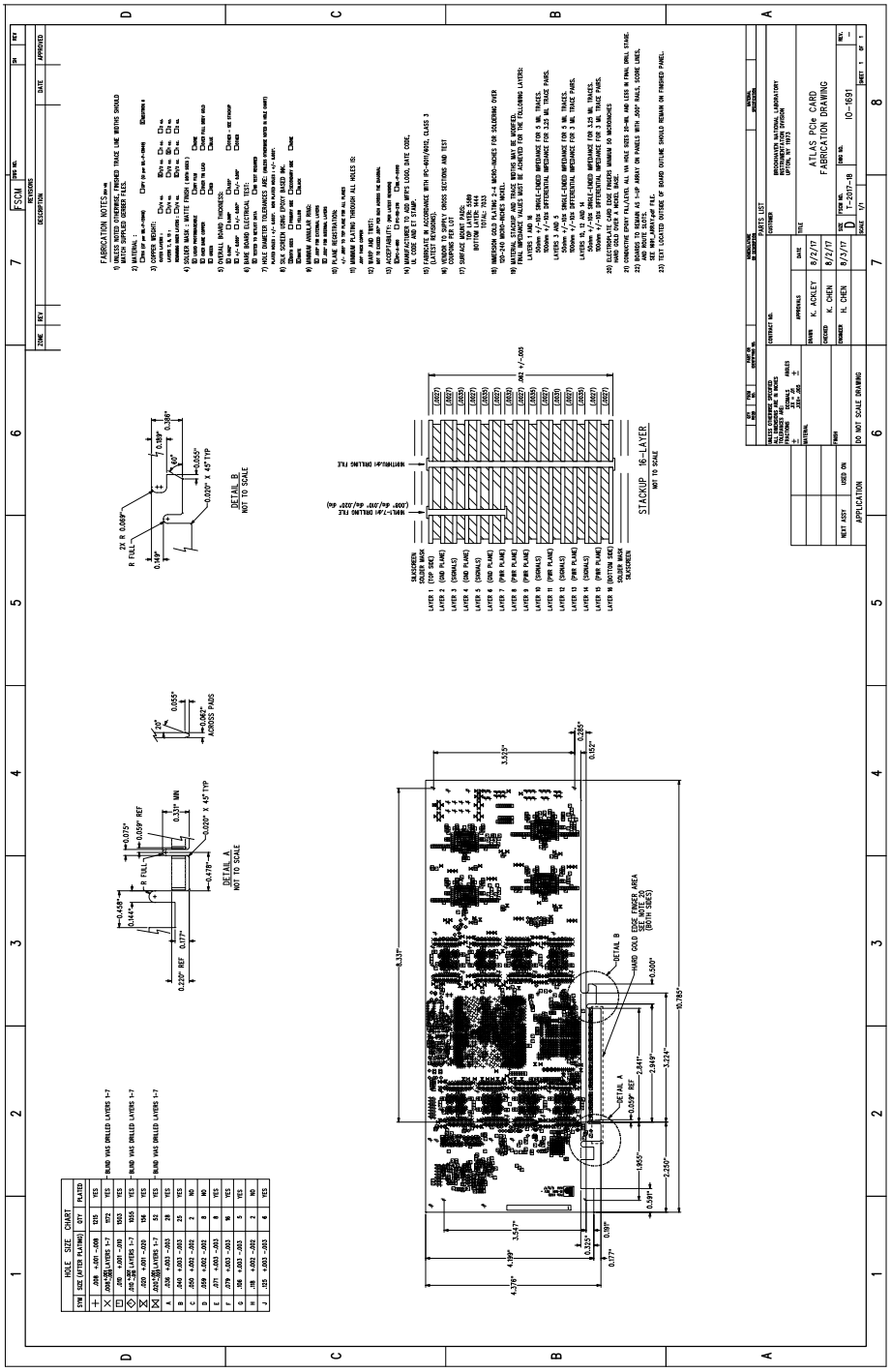


Figure 21: FLX-712 Fabrication Schematic and Stackup.

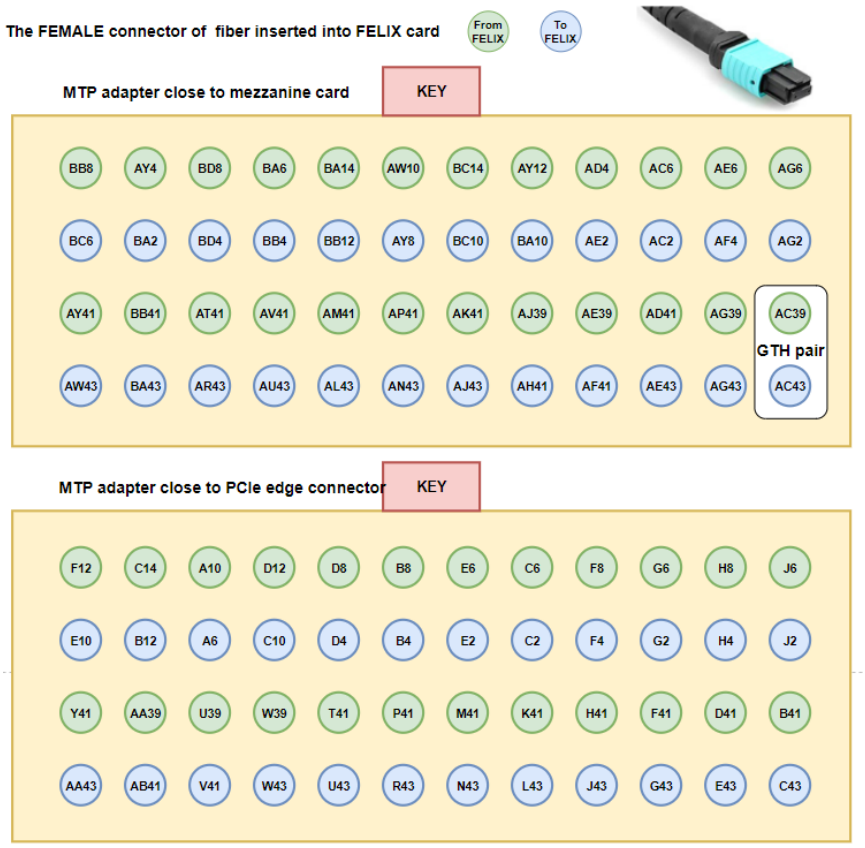


Figure 22: Mapping for external fiber to the GTH pins of FELIX FPGA: 48-ch version.

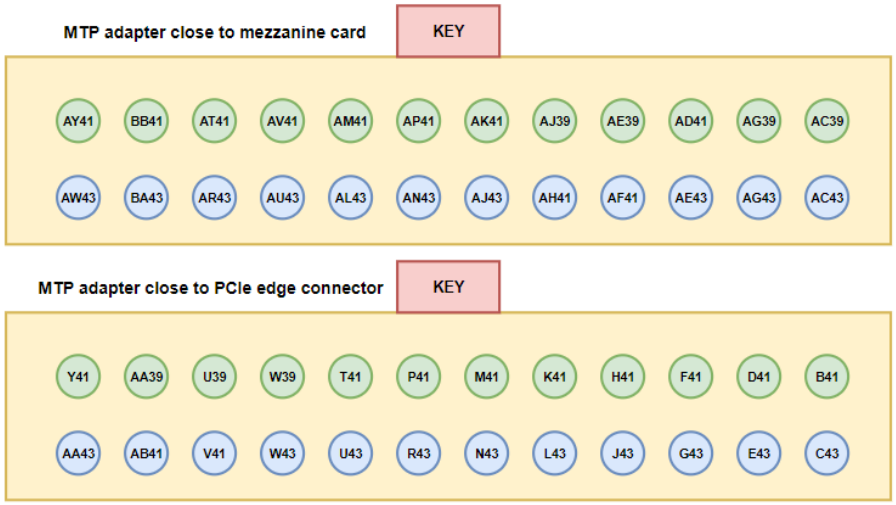


Figure 23: Mapping for external fiber to the GTH pins of FELIX FPGA: 24-ch version.

| GTH TX | GTH RX | MiniPOD Group | Firmware Channel: 48-ch mode | Firmware Channel: 8-ch mode | Firmware Channel: 16-ch mode | Firmware Channel: 24-ch mode |
|---|---|---|---|---|---|---|
| AG6/AG5 | AG2/AG1 | B | 12 | | | |
| AE6/AE5 | AF4/AF3 | B | 13 | | | |
| AC6/AC5 | AC2/AC1 | B | 14 | | | |
| AD4/AD3 | AE2/AE1 | B | 15 | | | |
| AY12/AY11 | BA10/BA9 | B | 16 | | | |
| BC14/BC13 | BC10/BC9 | B | 17 | | | |
| AW10/AW9 | AY8/AY7 | B | 18 | | | |
| BA14/BA13 | BB12/BB11 | B | 19 | | | |
| BA6/BA5 | BB4/BB3 | B | 20 | | | |
| BD8/BD7 | BD4/BD3 | B | 21 | | | |
| AY4/AY3 | BA2/BA1 | B | 22 | | | |
| BB8/BB7 | BC6/BC5 | B | 23 | | | |
| AC39/AC40 | AC43/AC44 | A | 0 | 0 | 0 | 0 |
| AG39/AG40 | AG43/AG44 | A | 1 | 1 | 1 | 1 |
| AD41/AD42 | AE43/AE44 | A | 2 | 2 | 2 | 2 |
| AE39/AE40 | AF41/AF42 | A | 3 | 3 | 3 | 3 |
| AJ39/AJ40 | AH41/AH42 | A | 4 | | 4 | 4 |
| AK41/AK42 | AJ43/AJ44 | A | 5 | | 5 | 5 |
| AP41/AP42 | AN43/AN44 | A | 6 | | 6 | 6 |
| AM41/AM42 | AL43/AL44 | A | 7 | | 7 | 7 |
| AV41/AV42 | AU43/AU44 | A | 8 | | | 8 |
| AT42/AT42 | AR43/AR44 | A | 9 | | | 9 |
| BB41/BB42 | BA43/BA44 | A | 10 | | | 10 |
| AY41/AY42 | AW43/AW44 | A | 11 | | | 11 |
| J6/J5 | J2/J1 | D | 36 | | | |
| H8/H7 | H4/H3 | D | 37 | | | |
| G6/G5 | G2/G1 | D | 38 | | | |
| F8/F7 | F4/F3 | D | 39 | | | |
| C6/C5 | C2/C1 | D | 40 | | | |
| E6/E5 | E2/E1 | D | 41 | | | |
| B8/B7 | B4/B3 | D | 42 | | | |
| D8/D7 | D4/D3 | D | 43 | | | |
| D12/D11 | C10/C9 | D | 44 | | | |
| A10/A9 | A6/A5 | D | 45 | | | |
| C14/C13 | B12/B11 | D | 46 | | | |
| F12/F11 | E10/E9 | D | 47 | | | |
| B41/B42 | C43/C44 | C | 24 | 4 | 8 | 12 |
| D41/D42 | E43/E44 | C | 25 | 5 | 9 | 13 |
| F41/F42 | G43/G44 | C | 26 | 6 | 10 | 14 |
| H41/H42 | J43/J44 | C | 27 | 7 | 11 | 15 |
| K41/K42 | L43/L44 | C | 28 | | 12 | 16 |
| M41/M42 | N43/N44 | C | 29 | | 13 | 17 |
| P41/P42 | R43/R44 | C | 30 | | 14 | 18 |
| T41/T42 | U43/U44 | C | 31 | | 15 | 19 |
| W39/W40 | W43/W44 | C | 32 | | | 20 |
| U39/U40 | V41/V42 | C | 33 | | | 21 |
| AA39/AA40 | AB41/AB42 | C | 34 | | | 22 |
| Y41/Y42 | AA43/AA44 | C | 35 | | | 23 |

Figure 24: Mapping between the GTH transceiver and firmware chanels.

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