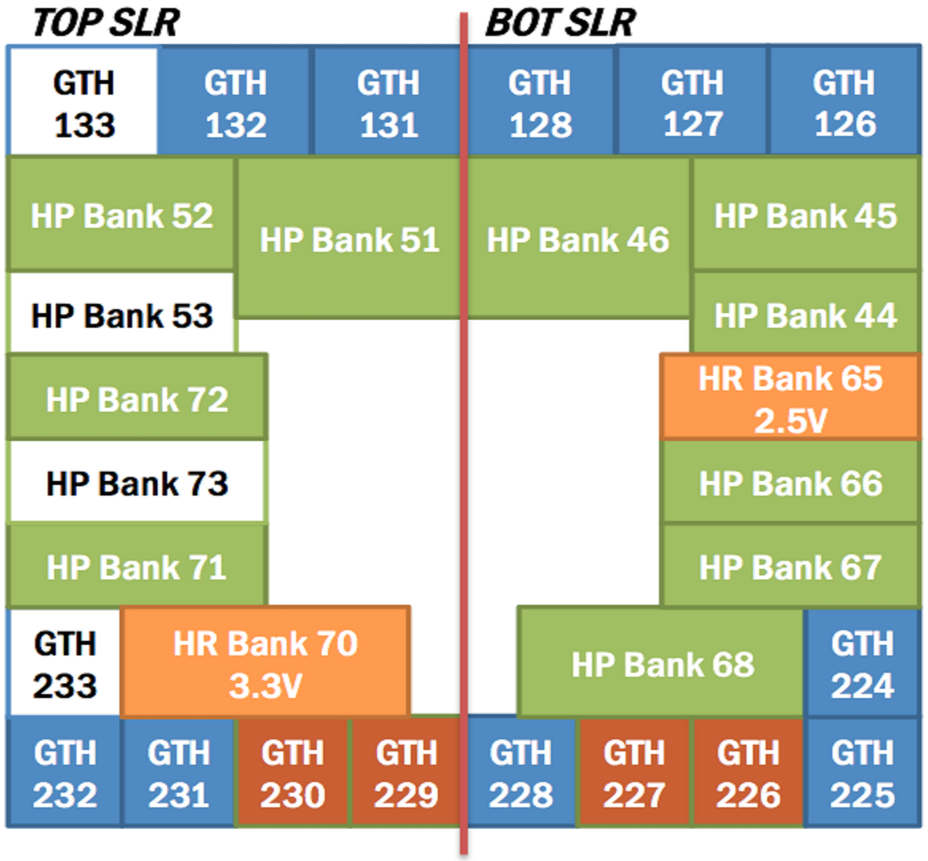


P2: CONFIGURATION

P3: JTAG FOR REMOTE

P4: ADR, TIMING MEZZANINE, SI5345 CONFIG

P5: THE 12 QUADS OF 48 TX/RX LINKS

P6: PCIE CNT & 4 GTH QUADS

P7: BANK 65 (2.5V HR) & BANK 66-68

P8: POWER & GND FOR FPGA

P9: CDR & CLOCKS

P10: PEX8732 STATIONS 0&1

P11: PEX8732 CONTROL & POWER PINS

P12: POWER: LTM4630A

P13: POWER: LTM4630A

P14: MINIPOD TX x4

P15: MINIPOD RX x4

P16: VOLTAGE/CURRENT/TEMPERATURE MONITOR & CNTS

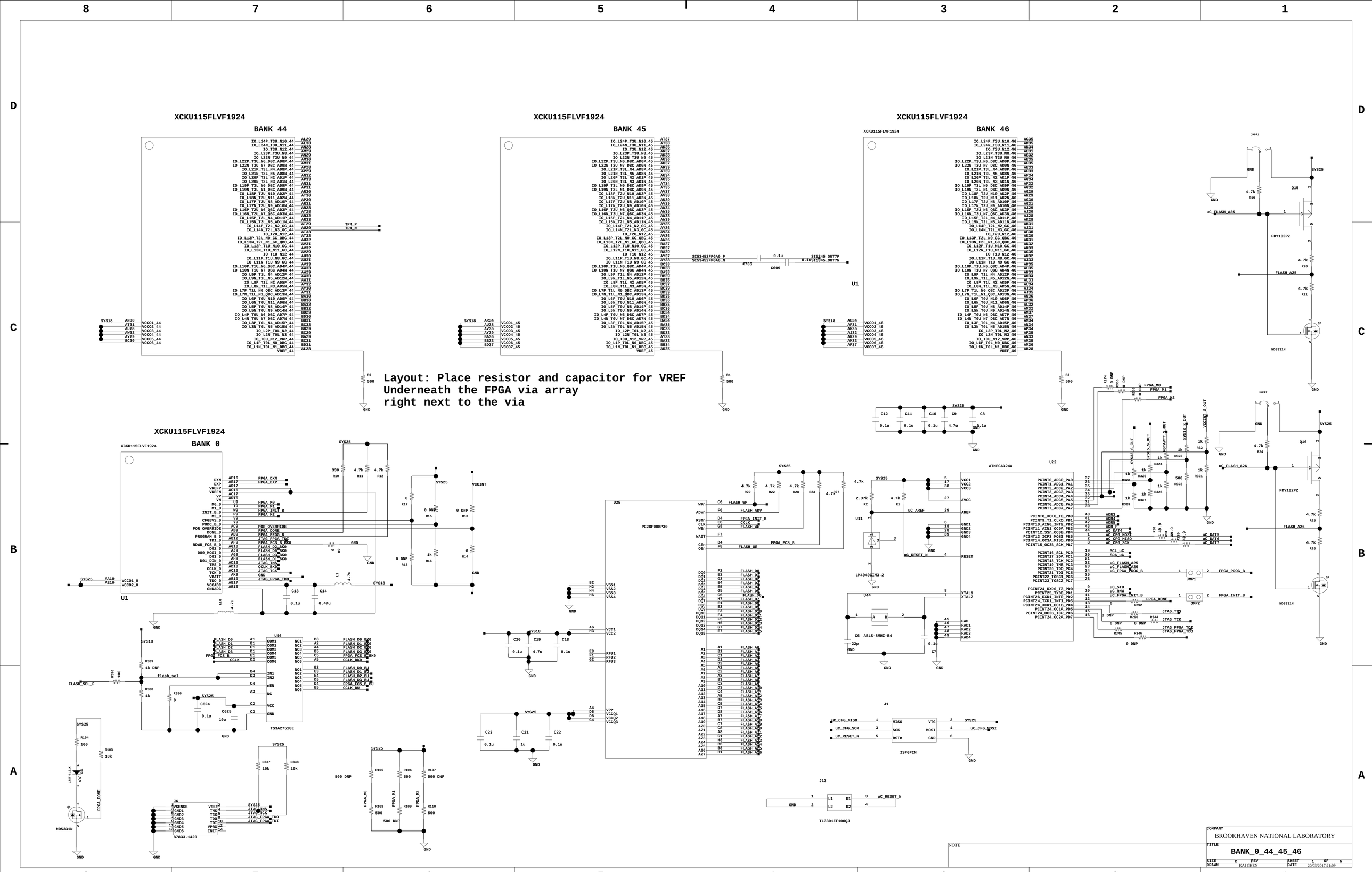
NOTE

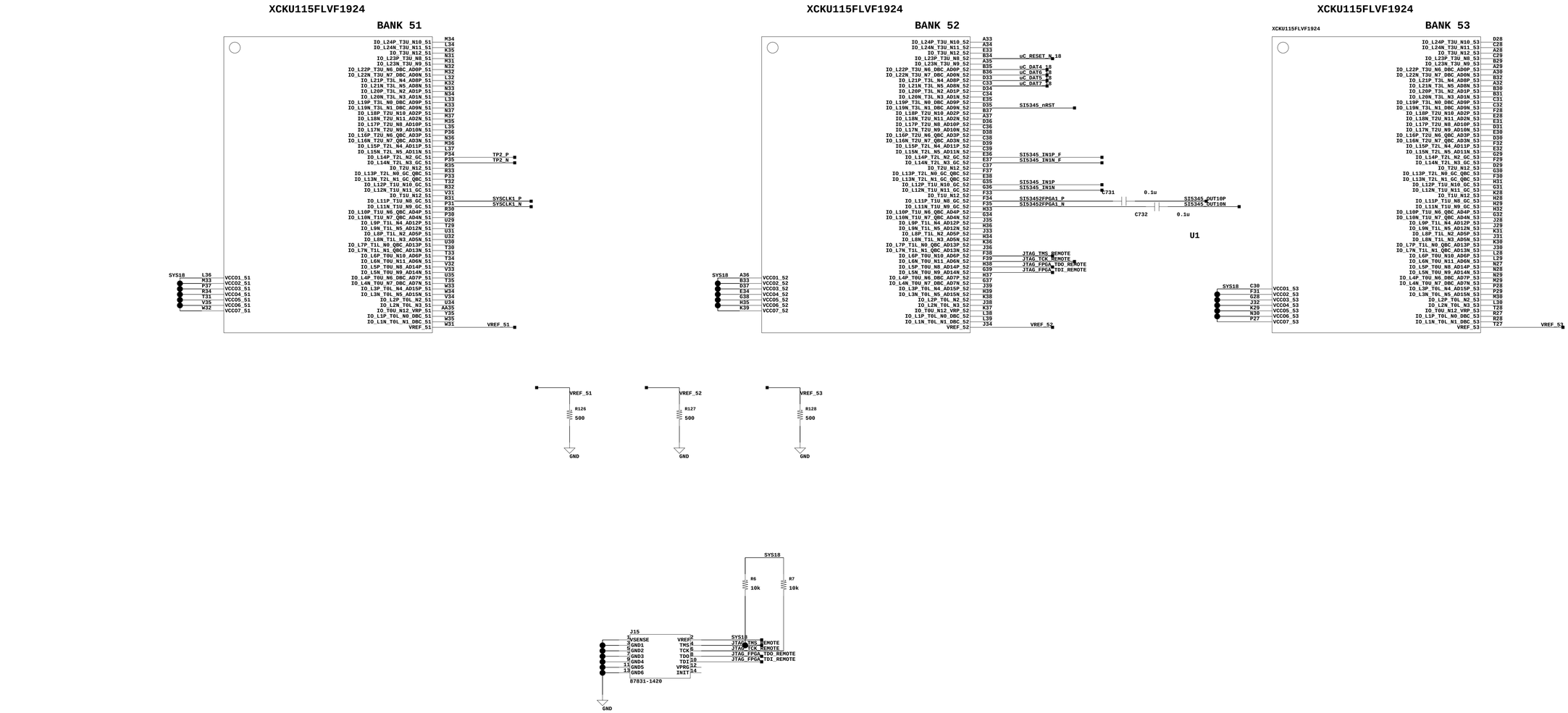
COMPANY BROOKHAVEN NATIONAL LABORATORY

TITLE

SIZE D REV SHEET TOP OF N

DRAWN KAI CHEN DATE 28/02/2017:10:43


XCKU115FLVF1924
BANK 44
XCKU115FLVF1924
BANK 45
XCKU115FLVF1924
BANK 46
Layout: Place resistor and capacitor for VREF
Underneath the FPGA via array
right next to the via
XCKU115FLVF1924
BANK 0
U1
U46
TS3A27518E
U25
PC28F00BP30
U22
ATMEGA324A
U11
LM4040CIM3-2
U44
ABLS-8MHZ-B4
U1
J1
ISP6PIN
J13
TL3301EF100QJ
J6
87833-1420
JMPR1
JMPR2
JMP1
JMP2
Q15
Q16
FDY102PZ
NDS331N
TP4_P
TP4_N
FPGA_DXN
FPGA_DXP
FPGA_M0
FPGA_M1
FPGA_INIT_B
FPGA_M2
FPGA_DONE
FPGA_CCLK
FPGA_PROG_B
FPGA_FCS_B
FPGA_D00_MOSI
FPGA_D01_DIN
FPGA_D02
FPGA_D03
FLASH_SEL_F
flash_sel
JTAG_FPGA_TDO
JTAG_FPGA_TDI
JTAG_TMS
JTAG_TCK
JTAG_FPGA_TDI
SIS3452FPGA0_P
SIS3452FPGA0_N
SIS345_OUT7P
SIS345_OUT7N
uC_RESET_N
uC_CFG_MISO
uC_CFG_SCK
uC_CFG_MOSI
uC_FLASH_A25
uC_FLASH_A26
uC_FPGA_PROG_B
uC_FPGA_INIT_B
uC_FLASH_A24
uC_DAT4
uC_DAT5
uC_DAT6
uC_DAT7
uC_STB
uC_RDWR
SCL_uC
SDA_uC
FLASH_A24
FLASH_A25
FLASH_A26
SYS25_S_OUT
SYS18_S_OUT
MEZAVTT_S_OUT
VCCINT_S_OUT
SYS25
SYS18
VCCINT
GND
0.1u
0.47u
4.7u
1k DNP
500 DNP
COMPANY
BROOKHAVEN NATIONAL LABORATORY
TITLE
BANK_0_44_45_46
SIZE D REV
SHEET 1 OF N
DRAWN KAI CHEN
DATE 20/03/2017:21:09
NOTE



NOTE

COMPANY BROOKHAVEN NATIONAL LABORATORY

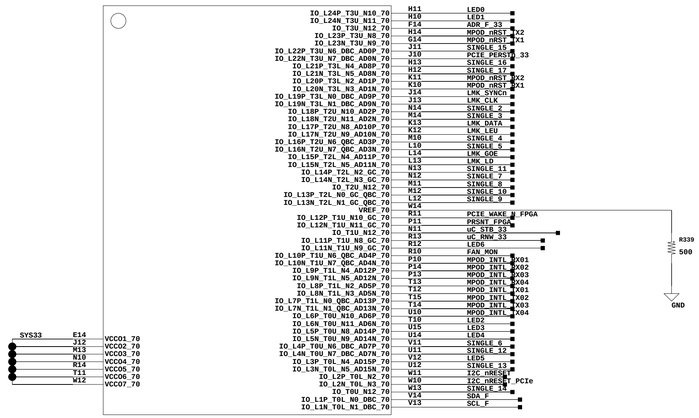
TITLE BANK_51_52_53

SIZE D REV SHEET OF N

DRAWN KAI CHEN DATE 24/03/2017 14:44

XCKU115FLVF1924

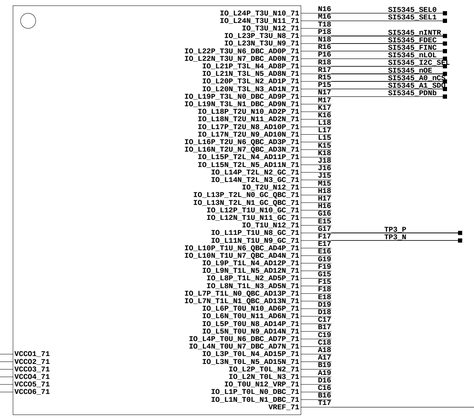
BANK 70



U1

XCKU115FLVF1924

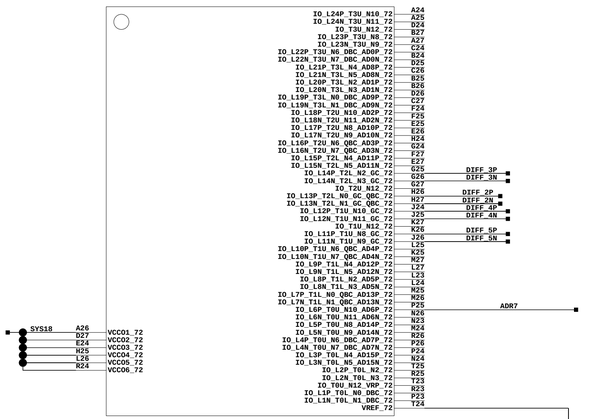
BANK 71



SYS18 A16 → VCCO1_71
VCCO2_71
VCCO3_71
VCCO4_71
VCCO5_71
VCCO6_71
P17

XCKU115FLVF1924

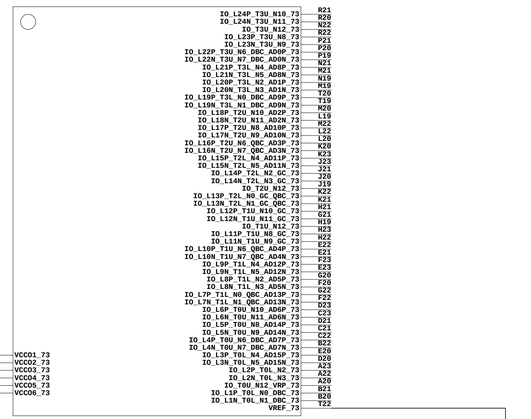
BANK 72



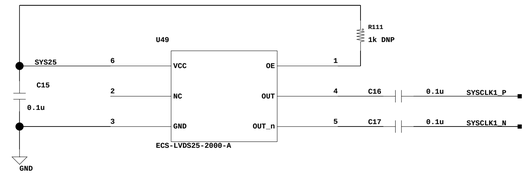
SYS18 A26 → VCCO1_72
VCCO2_72
VCCO3_72
VCCO4_72
VCCO5_72
VCCO6_72
D27
E24
N25
L26
N24

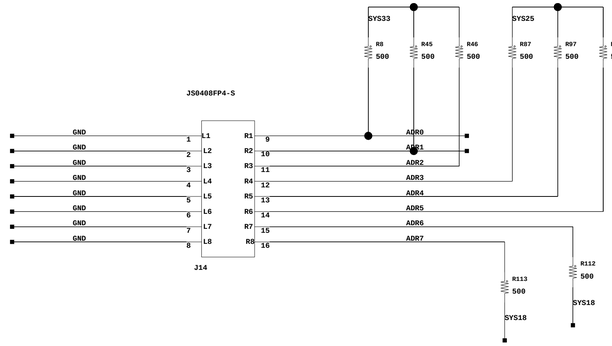
XCKU115FLVF1924

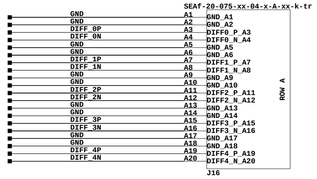
BANK 73

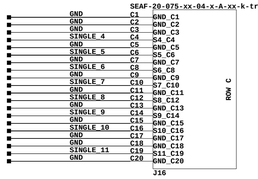


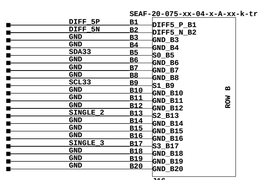
SYS18 B23 → VCCO1_73
VCCO2_73
VCCO3_73
VCCO4_73
VCCO5_73
VCCO6_73
C20
F21
J22
K19
T21

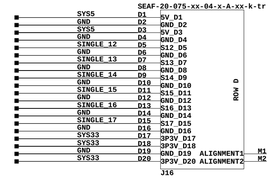






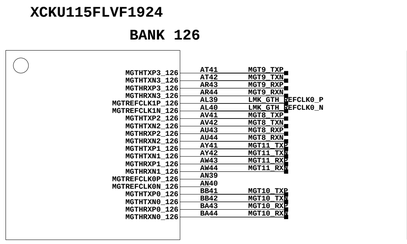


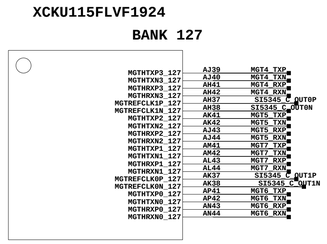


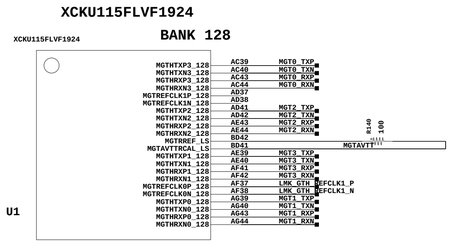


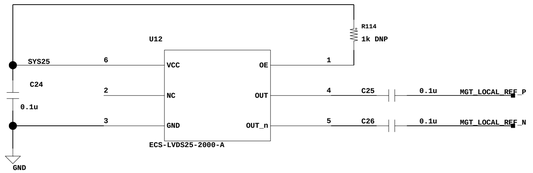
NOTE

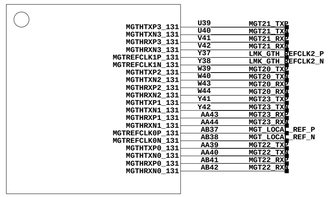
COMPANY	BROOKHAVEN NATIONAL LABORATORY
TITLE	BANK_70_71_72_73
SIZE	D
REV	
SHEET	OF N
DRAWN	KAI CHEN
DATE	21/03/2017:10:17

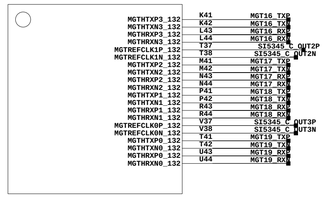


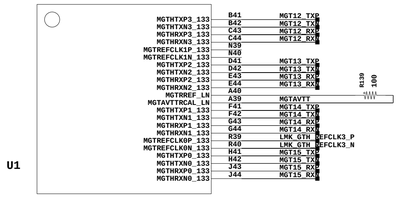


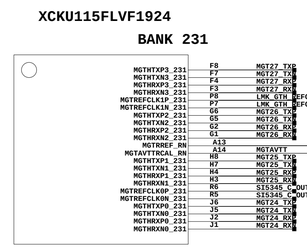


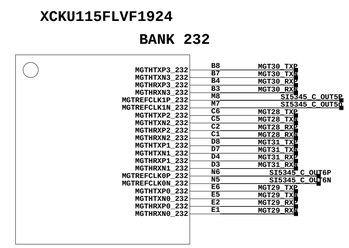


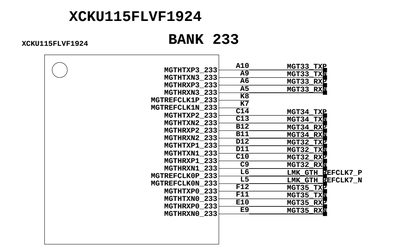


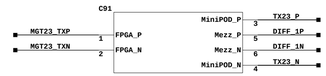












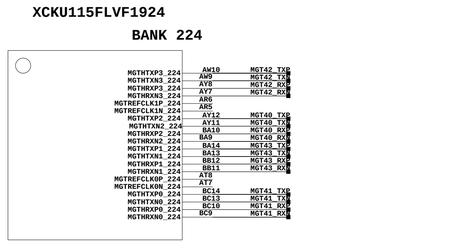
NOTE

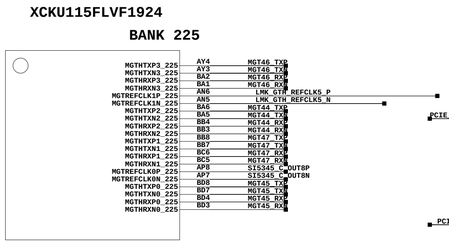
COMPANY BROOKHAVEN NATIONAL LABORATORY

TITLE GTH_FOR_DATA

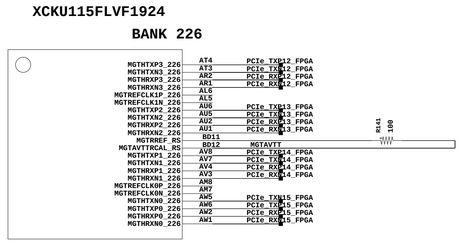
SIZE D REV SHEET OF N

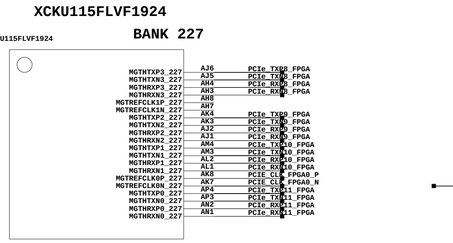
DRAWN KAI CHEN DATE 24/03/2017:14:44

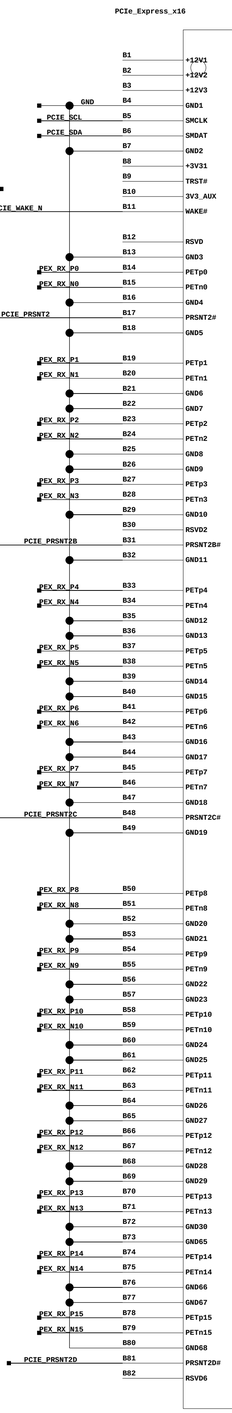




U1

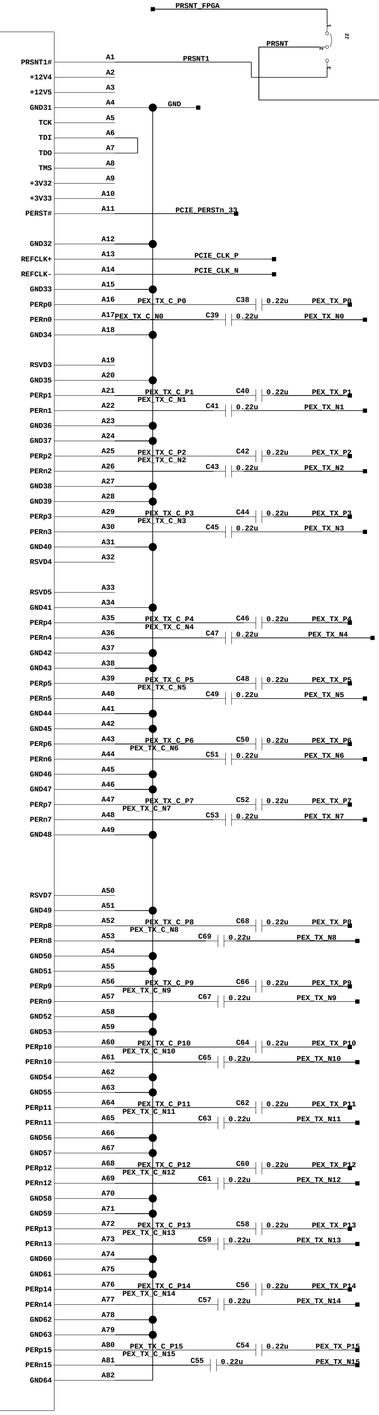


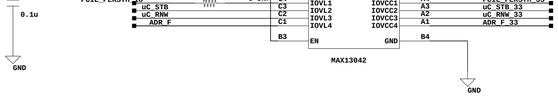


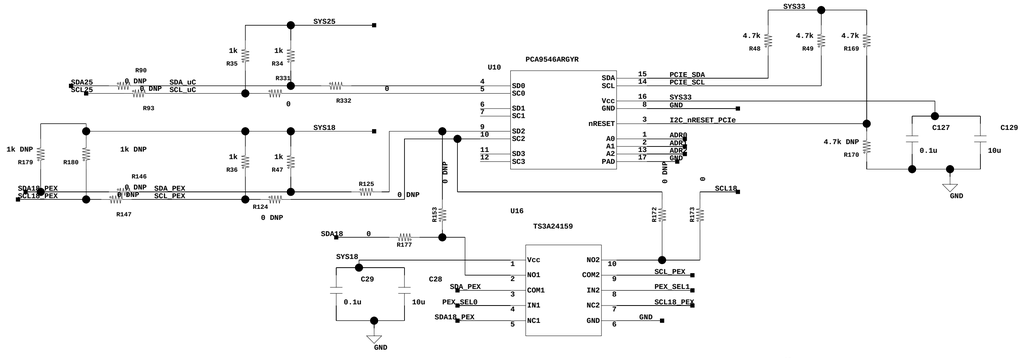


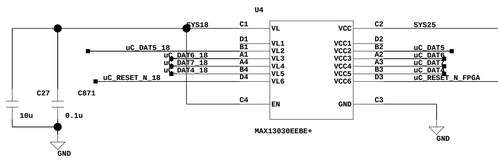
PCIe x16

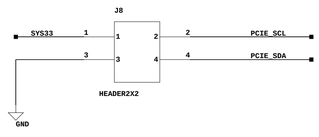
U45

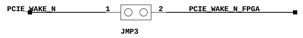












NOTE

COMPANY
BROOKHAVEN NATIONAL LABORATORY

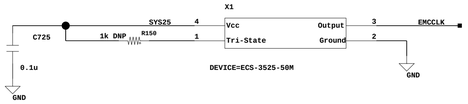
TITLE
PCIE GTH & EDGE

SIZE	D	REV	SHEET	OF	N
DRAWN	KAI CHEN		DATE	21/03/2017:10:37	

Layout: Place resistor and capacitor for VREF

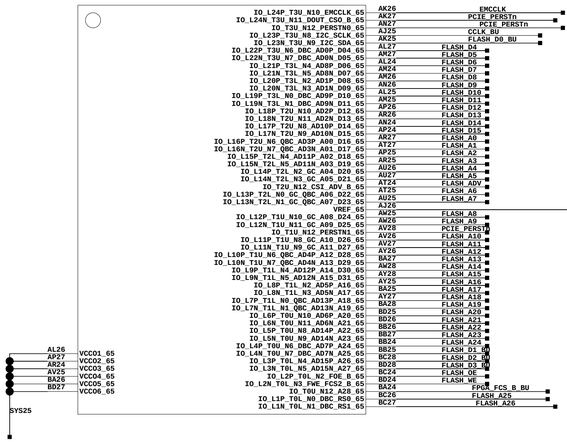
Underneath the FPGA via array

right next to the via



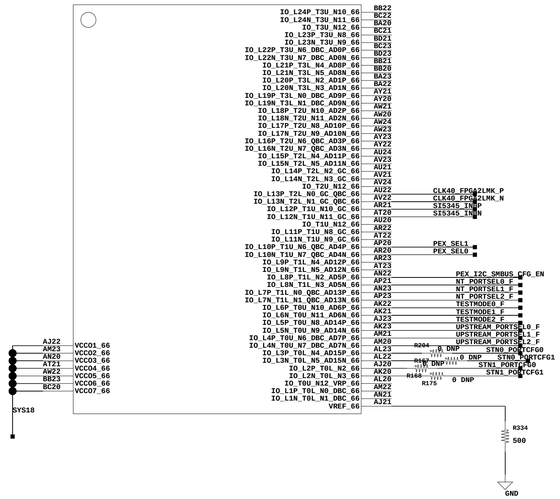
XCKU115FLVF1924

BANK 65



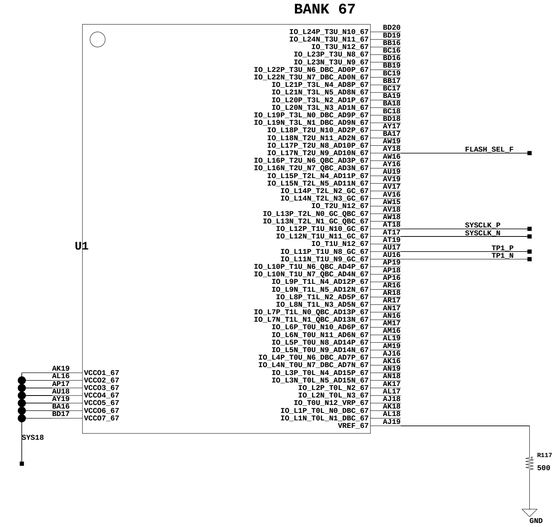
XCKU115FLVF1924

BANK 66



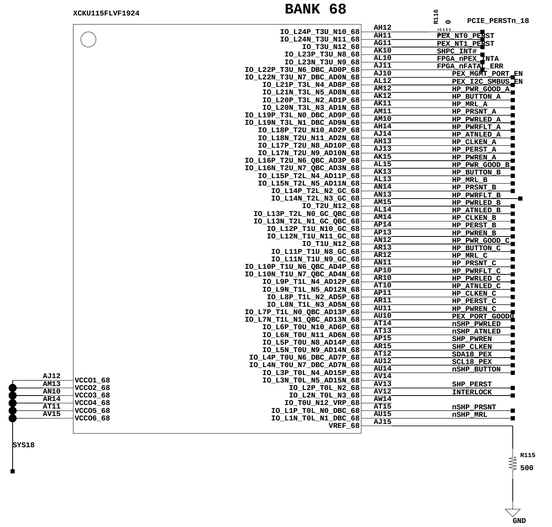
XCKU115FLVF1924

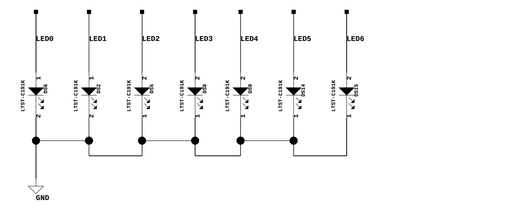
BANK 67

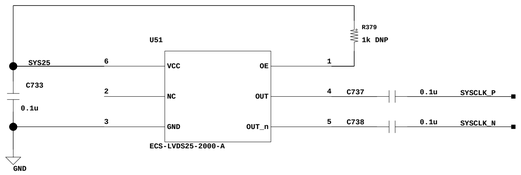


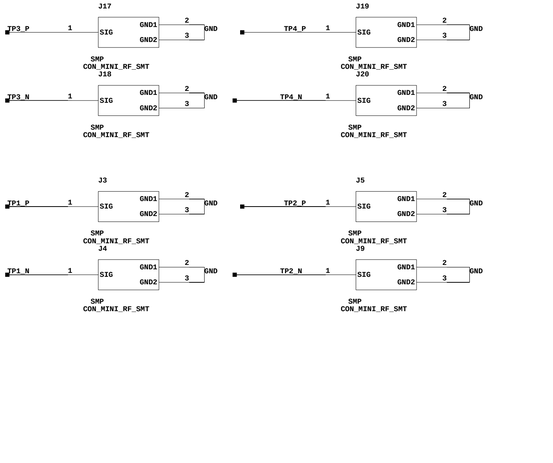
XCKU115FLVF1924

BANK 68



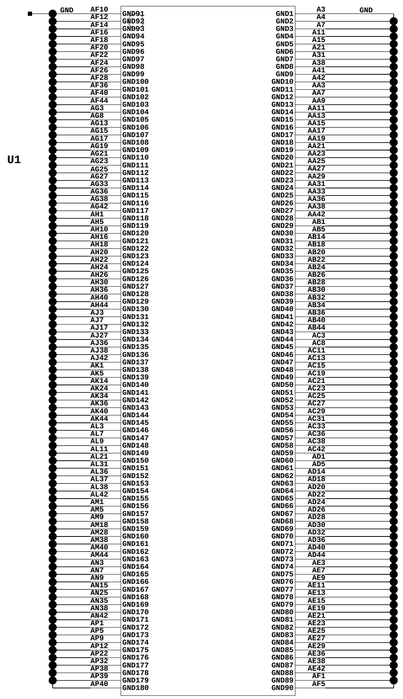






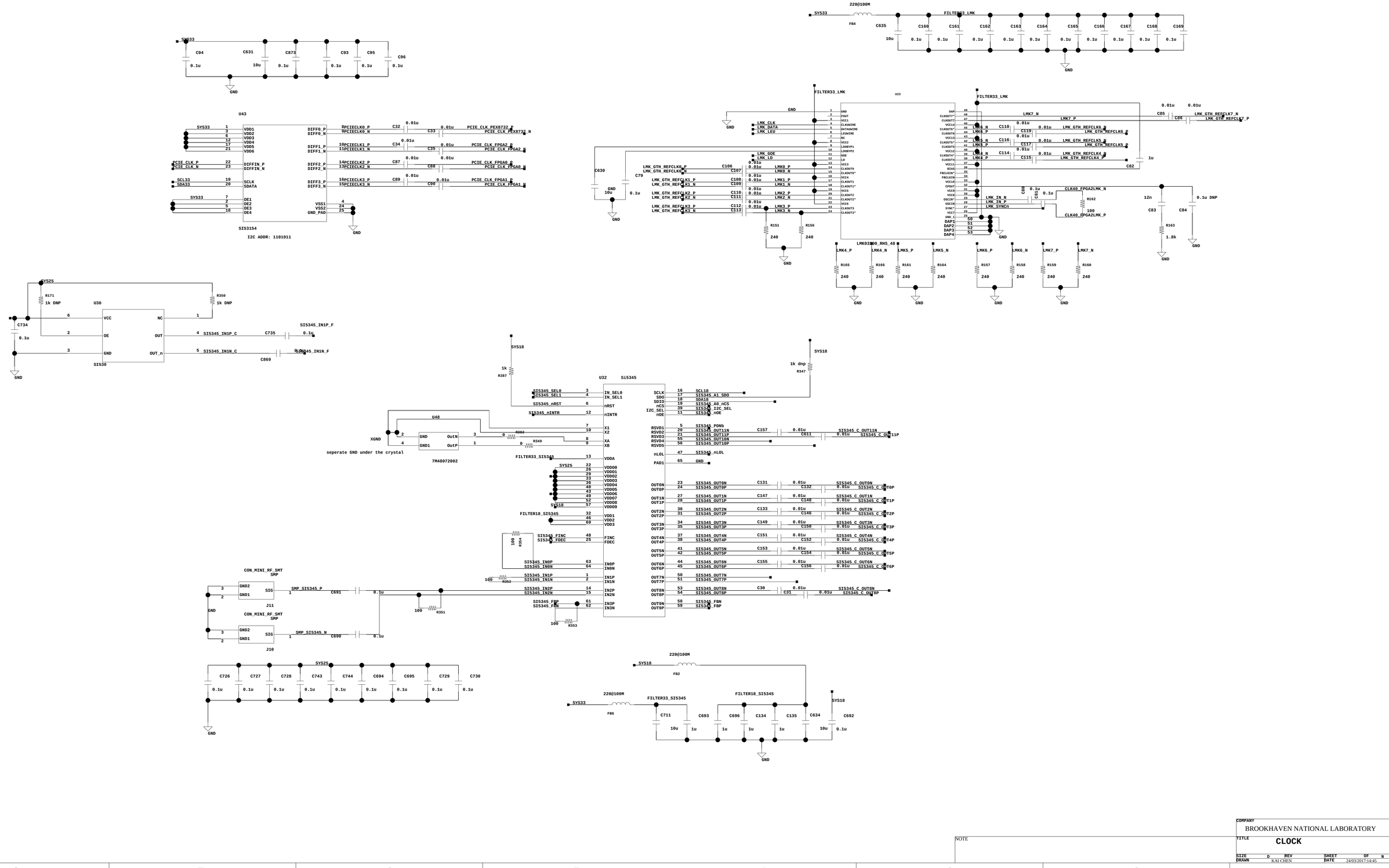
NOTE

COMPANY	BROOKHAVEN NATIONAL LABORATORY
TITLE	BANK_65_66_67_68
SIZE D REV	SHEET OF N
DRAWN KAI CHEN	DATE 20/03/2017 21:14



COMPANY	BROOKHAVEN NATIONAL LABORATORY
TITLE	FPGA_POWER_PINS
SIZE	D
REV	
SHEET	
OF	N
DRAWN	KAI CHEN
DATE	28/02/2017:11:12

NOTE



NOTE

COMPANY	BROOKHAVEN NATIONAL LABORATORY
TITLE	CLOCK
SIZE D REV	SHEET OF N
DRAWN KAI CHEN	DATE 24/03/2017:14:45

PEX8732

U31

Station 0

PEX8732

R188 3k — REXT_A0
R189 3k — REXT_B0
R190 3k — REXT_A1
R191 3k — REXT_B1
R192 3k — REXT_A2
R193 3k — REXT_B2
R194 3k — REXT_A3
R195 3k — REXT_B3
R357 3k — REXT_CMU
GND

PCIE_CLK_PEX8732_P — AE9 — PEX_REFCLKp
PCIE_CLK_PEX8732_N — AF9 — PEX_REFCLKn

PEX_PETp[0]	AE5	PEX_TX_P0	
PEX_PETn[0]	AF5	PEX_TX_N0	
PEX_PERp[0]	AB5	PEX_RX_P0	
PEX_PERn[0]	AC5	PEX_RX_N0	
PEX_PETp[1]	AE6	PEX_TX_P1	
PEX_PETn[1]	AF6	PEX_TX_N1	
PEX_PERp[1]	AB6	PEX_RX_P1	
PEX_PERn[1]	AC6	PEX_RX_N1	
PEX_PETp[2]	AE7	PEX_TX_P2	
PEX_PETn[2]	AF7	PEX_TX_N2	
PEX_PERp[2]	AB7	PEX_RX_P2	
PEX_PERn[2]	AC7	PEX_RX_N2	
PEX_PETp[3]	AE8	PEX_TX_P3	
PEX_PETn[3]	AF8	PEX_TX_N3	
PEX_PERp[3]	AB8	PEX_RX_P3	
PEX_PERn[3]	AC8	PEX_RX_N3	
PEX_PETp[4]	AE10	PEX_TX_P4	
PEX_PETn[4]	AF10	PEX_TX_N4	
PEX_PERp[4]	AB10	PEX_RX_P4	
PEX_PERn[4]	AC10	PEX_RX_N4	
PEX_PETp[5]	AE11	PEX_TX_P5	
PEX_PETn[5]	AF11	PEX_TX_N5	
PEX_PERp[5]	AB11	PEX_RX_P5	
PEX_PERn[5]	AC11	PEX_RX_N5	
PEX_PETp[6]	AE12	PEX_TX_P6	
PEX_PETn[6]	AF12	PEX_TX_N6	
PEX_PERp[6]	AB12	PEX_RX_P6	
PEX_PERn[6]	AC12	PEX_RX_N6	
PEX_PETp[7]	AE13	PEX_TX_P7	
PEX_PETn[7]	AF13	PEX_TX_N7	
PEX_PERp[7]	AB13	PEX_RX_P7	
PEX_PERn[7]	AC13	PEX_RX_N7	
PEX_PETp[8]	AE14	PEX_TX_P8	
PEX_PETn[8]	AF14	PEX_TX_N8	
PEX_PERp[8]	AB14	PEX_RX_P8	
PEX_PERn[8]	AC14	PEX_RX_N8	
PEX_PETp[9]	AE15	PEX_TX_P9	
PEX_PETn[9]	AF15	PEX_TX_N9	
PEX_PERp[9]	AB15	PEX_RX_P9	
PEX_PERn[9]	AC15	PEX_RX_N9	
PEX_PETp[10]	AE16	PEX_TX_P10	
PEX_PETn[10]	AF16	PEX_TX_N10	
PEX_PERp[10]	AB16	PEX_RX_P10	
PEX_PERn[10]	AC16	PEX_RX_N10	
PEX_PETp[11]	AE17	PEX_TX_P11	
PEX_PETn[11]	AF17	PEX_TX_N11	
PEX_PERp[11]	AB17	PEX_RX_P11	
PEX_PERn[11]	AC17	PEX_RX_N11	
PEX_PETp[12]	AE19	PEX_TX_P12	
PEX_PETn[12]	AF19	PEX_TX_N12	
PEX_PERp[12]	AB19	PEX_RX_P12	
PEX_PERn[12]	AC19	PEX_RX_N12	
PEX_PETp[13]	AE20	PEX_TX_P13	
PEX_PETn[13]	AF20	PEX_TX_N13	
PEX_PERp[13]	AB20	PEX_RX_P13	
PEX_PERn[13]	AC20	PEX_RX_N13	
PEX_PETp[14]	AE21	PEX_TX_P14	
PEX_PETn[14]	AF21	PEX_TX_N14	
PEX_PERp[14]	AB21	PEX_RX_P14	
PEX_PERn[14]	AC21	PEX_RX_N14	
PEX_PETp[15]	AE22	PEX_TX_P15	
PEX_PETn[15]	AF22	PEX_TX_N15	
PEX_PERp[15]	AB22	PEX_RX_P15	
PEX_PERn[15]	AC22	PEX_RX_N15	

PEX8732

U31

Station 1

PEX8732

R196 3k — REXT_A4
R197 3k — REXT_B4
R198 3k — REXT_A5
R199 3k — REXT_B5
R200 3k — REXT_A6
R201 3k — REXT_B6
R202 3k — REXT_A7
R203 3k — REXT_B7
GND

W1 — NC14
W2 — NC15
N2 — NC16
N1 — NC17
F1 — NC18
E1 — NC19
B9 — NC20
A9 — NC21

PEX_PETp[16]	U2	PEX_F_R0_P	C178	0.22u	PCIe_RXP0_FPGA
PEX_PETn[16]	U1	PEX_F_R0_N	C179	0.22u	PCIe_RXN0_FPGA
PEX_PERp[16]	U5	PEX_F_T0_P	C180	0.22u	PCIe_TXP0_FPGA
PEX_PERn[16]	U4	PEX_F_T0_N	C181	0.22u	PCIe_TXN0_FPGA
PEX_PETp[17]	T2	PEX_F_R1_P	C182	0.22u	PCIe_RXP1_FPGA
PEX_PETn[17]	T1	PEX_F_R1_N	C183	0.22u	PCIe_RXN1_FPGA
PEX_PERp[17]	T5	PEX_F_T1_P	C184	0.22u	PCIe_TXP1_FPGA
PEX_PERn[17]	T4	PEX_F_T1_N	C185	0.22u	PCIe_TXN1_FPGA
PEX_PETp[18]	R2	PEX_F_R2_P	C186	0.22u	PCIe_RXP2_FPGA
PEX_PETn[18]	R1	PEX_F_R2_N	C187	0.22u	PCIe_RXN2_FPGA
PEX_PERp[18]	R5	PEX_F_T2_P	C188	0.22u	PCIe_TXP2_FPGA
PEX_PERn[18]	R4	PEX_F_T2_N	C189	0.22u	PCIe_TXN2_FPGA
PEX_PETp[19]	P2	PEX_F_R3_P	C190	0.22u	PCIe_RXP3_FPGA
PEX_PETn[19]	P1	PEX_F_R3_N	C191	0.22u	PCIe_RXN3_FPGA
PEX_PERp[19]	P5	PEX_F_T3_P	C192	0.22u	PCIe_TXP3_FPGA
PEX_PERn[19]	P4	PEX_F_T3_N	C193	0.22u	PCIe_TXN3_FPGA
PEX_PETp[20]	M2	PEX_F_R4_P	C194	0.22u	PCIe_RXP4_FPGA
PEX_PETn[20]	M1	PEX_F_R4_N	C195	0.22u	PCIe_RXN4_FPGA
PEX_PERp[20]	M5	PEX_F_T4_P	C196	0.22u	PCIe_TXP4_FPGA
PEX_PERn[20]	M4	PEX_F_T4_N	C197	0.22u	PCIe_TXN4_FPGA
PEX_PETp[21]	L2	PEX_F_R5_P	C198	0.22u	PCIe_RXP5_FPGA
PEX_PETn[21]	L1	PEX_F_R5_N	C199	0.22u	PCIe_RXN5_FPGA
PEX_PERp[21]	L5	PEX_F_T5_P	C200	0.22u	PCIe_TXP5_FPGA
PEX_PERn[21]	L4	PEX_F_T5_N	C201	0.22u	PCIe_TXN5_FPGA
PEX_PETp[22]	K2	PEX_F_R6_P	C202	0.22u	PCIe_RXP6_FPGA
PEX_PETn[22]	K1	PEX_F_R6_N	C203	0.22u	PCIe_RXN6_FPGA
PEX_PERp[22]	K5	PEX_F_T6_P	C204	0.22u	PCIe_TXP6_FPGA
PEX_PERn[22]	K4	PEX_F_T6_N	C205	0.22u	PCIe_TXN6_FPGA
PEX_PETp[23]	J2	PEX_F_R7_P	C206	0.22u	PCIe_RXP7_FPGA
PEX_PETn[23]	J1	PEX_F_R7_N	C207	0.22u	PCIe_RXN7_FPGA
PEX_PERp[23]	J5	PEX_F_T7_P	C208	0.22u	PCIe_TXP7_FPGA
PEX_PERn[23]	J4	PEX_F_T7_N	C209	0.22u	PCIe_TXN7_FPGA
PEX_PETp[24]	B5	PEX_F_R8_P	C171	0.22u	PCIe_RXP8_FPGA
PEX_PETn[24]	A5	PEX_F_R8_N	C172	0.22u	PCIe_RXN8_FPGA
PEX_PERp[24]	E5	PEX_F_T8_P	C170	0.22u	PCIe_TXP8_FPGA
PEX_PERn[24]	D5	PEX_F_T8_N	C172	0.22u	PCIe_TXN8_FPGA
PEX_PETp[25]	B6	PEX_F_R9_P	C210	0.22u	PCIe_RXP9_FPGA
PEX_PETn[25]	A6	PEX_F_R9_N	C211	0.22u	PCIe_RXN9_FPGA
PEX_PERp[25]	E6	PEX_F_T9_P	C212	0.22u	PCIe_TXP9_FPGA
PEX_PERn[25]	D6	PEX_F_T9_N	C213	0.22u	PCIe_TXN9_FPGA
PEX_PETp[26]	B7	PEX_F_R10_P	C214	0.22u	PCIe_RXP10_FPGA
PEX_PETn[26]	A7	PEX_F_R10_N	C215	0.22u	PCIe_RXN10_FPGA
PEX_PERp[26]	E7	PEX_F_T10_P	C216	0.22u	PCIe_TXP10_FPGA
PEX_PERn[26]	D7	PEX_F_T10_N	C217	0.22u	PCIe_TXN10_FPGA
PEX_PETp[27]	B8	PEX_F_R11_P	C218	0.22u	PCIe_RXP11_FPGA
PEX_PETn[27]	A8	PEX_F_R11_N	C219	0.22u	PCIe_RXN11_FPGA
PEX_PERp[27]	E8	PEX_F_T11_P	C220	0.22u	PCIe_TXP11_FPGA
PEX_PERn[27]	D8	PEX_F_T11_N	C221	0.22u	PCIe_TXN11_FPGA
PEX_PETp[28]	B10	PEX_F_R12_P	C222	0.22u	PCIe_RXP12_FPGA
PEX_PETn[28]	A10	PEX_F_R12_N	C223	0.22u	PCIe_RXN12_FPGA
PEX_PERp[28]	E10	PEX_F_T12_P	C224	0.22u	PCIe_TXP12_FPGA
PEX_PERn[28]	D10	PEX_F_T12_N	C225	0.22u	PCIe_TXN12_FPGA
PEX_PETp[29]	B11	PEX_F_R13_P	C226	0.22u	PCIe_RXP13_FPGA
PEX_PETn[29]	A11	PEX_F_R13_N	C227	0.22u	PCIe_RXN13_FPGA
PEX_PERp[29]	E11	PEX_F_T13_P	C228	0.22u	PCIe_TXP13_FPGA
PEX_PERn[29]	D11	PEX_F_T13_N	C229	0.22u	PCIe_TXN13_FPGA
PEX_PETp[30]	B12	PEX_F_R14_P	C230	0.22u	PCIe_RXP14_FPGA
PEX_PETn[30]	A12	PEX_F_R14_N	C231	0.22u	PCIe_RXN14_FPGA
PEX_PERp[30]	E12	PEX_F_T14_P	C232	0.22u	PCIe_TXP14_FPGA
PEX_PERn[30]	D12	PEX_F_T14_N	C233	0.22u	PCIe_TXN14_FPGA
PEX_PETp[31]	B13	PEX_F_R15_P	C174	0.22u	PCIe_RXP15_FPGA
PEX_PETn[31]	A13	PEX_F_R15_N	C175	0.22u	PCIe_RXN15_FPGA
PEX_PERp[31]	E13	PEX_F_T15_P	C176	0.22u	PCIe_TXP15_FPGA
PEX_PERn[31]	D13	PEX_F_T15_N	C177	0.22u	PCIe_TXN15_FPGA

PEX8732

U31

NC

PEX8732

Y25 — NC30
Y23 — NC31
N23 — NC32
N22 — NC33
E24 — NC34
F18 — NC35
D18 — NC36
E18 — NC37
W24 — NC22
W25 — NC23
N25 — NC24
N26 — NC25
B24 — NC26
A24 — NC27
B18 — NC28
A18 — NC29

NC38	U25	NC70	A22
NC39	U26	NC71	E22
NC40	U22	NC72	C22
NC41	U23	NC73	D22
NC42	T25	NC74	B21
NC43	T26	NC75	A21
NC44	T22	NC76	E21
NC45	T23	NC77	D21
NC46	R25	NC78	B20
NC47	R26	NC79	A20
NC48	R22	NC80	E20
NC49	R23	NC81	D20
NC50	P25	NC82	B19
NC51	P26	NC83	A19
NC52	P22	NC84	E19
NC53	P23	NC85	D19
NC54	N25	NC86	B17
NC55	N26	NC87	A17
NC56	M22	NC88	E17
NC57	M23	NC89	D17
NC58	L25	NC90	B16
NC59	L26	NC91	A16
NC60	L22	NC92	E16
NC61	L23	NC93	D16
NC62	K25	NC94	B15
NC63	K26	NC95	A15
NC64	K22	NC96	E15
NC65	K23	NC97	D15
NC66	J25	NC98	B14
NC67	J26	NC99	A14
NC68	J22	NC100	E14
NC69	J23	NC101	D14

NOTE

COMPANY: BROOKHAVEN NATIONAL LABORATORY
TITLE: PEX_STATIONS
SIZE: D | REV | SHEET | OF | N
DRAWN: KAI CHEN | DATE: 24/03/2017:14:36

PEX8732

U31

CONTROL

PEX8732

SYS1V8

PCIE_PERSTn_18
PEX_NTB_PERST
PEX_NT1_PERST

SHPC_INT#
FPGA_nPEX_INTA
FPGA_nFATAL_ERR

R234 1k PEX_JTAG_RSTn

TESTMODE0
TESTMODE1
TESTMODE2

UPSTREAM_PORTSEL0
UPSTREAM_PORTSEL1
UPSTREAM_PORTSEL2

STN0_PORTCFG0
STN0_PORTCFG1

STN1_PORTCFG0
STN1_PORTCFG1

PEX_MGMT_PORT_EN

R207 0

PEX_I2C_SMBUS_CFG_EN

R208 0 DNP

ADR6

PEX_I2C_SMBUS_EN

NT_PORTSEL0
NT_PORTSEL1
NT_PORTSEL2

GEN1_GEN2

HP_PWR_GOOD_A_VS_MODE	W21	HP_PWR_GOOD_A
HP_BUTTON_A_VS0_PERST#	Y24	HP_BUTTON_A
HP_MRL_A#_VS1_PERST#	AB26	HP_MRL_A
HP_PRSNT_A#_VS2_PERST#	AB26	HP_PRSNT_A
HP_PWRFLT_A#_VS1_FATAL_ERR#	AE26	HP_PWRFLT_A
HP_PWRLED_A#_VS0_FATAL_ERR#	Y23	HP_PWRLED_A
HP_ATNLED_A#_VS0_PEX_INTA#	AC26	HP_ATNLED_A
HP_CLKEN_A#_VS1_PEX_INTA#	AA24	HP_CLKEN_A
HP_PERST_A#_VS2_PEX_INTA#	AB25	HP_PERST_A
HP_PWREN_A_VS2_FATAL_ERR#	W22	HP_PWREN_A
HP_PWR_GOOD_B_PORT_GOOD7#	Y3	HP_PWR_GOOD_B
HP_BUTTON_B#_PORT_GOOD2#	AB3	HP_BUTTON_B
HP_MRL_B#_PORT_GOOD4#	AB2	HP_MRL_B
HP_PRSNT_B#_PORT_GOOD6#	W5	HP_PRSNT_B
HP_PWRFLT_B#_PORT_GOOD9#	AC3	HP_PWRFLT_B
HP_PWRLED_B#_PORT_GOOD10#	AD2	HP_PWRLED_B
HP_ATNLED_B#_PORT_GOOD1#	AB1	HP_ATNLED_B
HP_CLKEN_B#_PORT_GOOD3#	AE1	HP_CLKEN_B
HP_PERST_B#_PORT_GOOD5#	AD1	HP_PERST_B
HP_PWREN_B_PORT_GOOD8#	AC2	HP_PWREN_B
HP_PWR_GOOD_C_PORT_GOOD11#	F25	HP_PWR_GOOD_C
HP_BUTTON_C#_VS3_PERST#	C25	HP_BUTTON_C
HP_MRL_C#_VS4_PERST#	G21	HP_MRL_C
HP_PRSNT_C#_VS5_PERST#	D25	HP_PRSNT_C
HP_PWRFLT_C#_VS4_FATAL_ERR#	B26	HP_PWRFLT_C
HP_PWRLED_C#_VS3_FATAL_ERR#	D26	HP_PWRLED_C
HP_ATNLED_C#_VS3_PEX_INTA#	B25	HP_ATNLED_C
HP_CLKEN_C#_VS4_PEX_INTA#	F24	HP_CLKEN_C
HP_PERST_C#_VS5_PEX_INTA#	G22	HP_PERST_C
HP_PWREN_C_VS5_FATAL_ERR#	D24	HP_PWREN_C

PORT_GOOD0#	D3	PEX_PORT_GOOD0
I2C_SDA1	AE25	PEX_MASTER_SDA
I2C_SCL1	AC25	PEX_MASTER_SCL
I2C_SDA0	E3	SDA_PEX
I2C_SCL0	G4	SCL_PEX
NC1	Y2	
NC2	AA9	
NC3	F9	
NC4	W4	
SPARE0	D2	
SPARE1	AA3	
SPARE2	AA2	
SPARE3	AA1	
THERMAL_DIODEn	AC24	PEX_DIODE_N
THERMAL_DIODEp	AF25	PEX_DIODE_P

PEX_PERSTn	AC1	PEX_PERST#
PEX_NT_PERST	AD25	PEX_NT_PERST#
NC5	F3	
SHPC_INT#	B3	SHPC_INT#
PEX_INTA#	D1	PEX_INTA#
FATAL_ERR#	C24	
JTAG_TRST#	C2	
JTAG_TCK	B2	
JTAG_TMS	B1	
JTAG_TDI	C3	
JTAG_TDO	G5	
EE_SK	E25	
EE_CS#	E26	
EE_DI	G23	
EE_DO	F26	
STRAP_TESTMODE0	Y6	
STRAP_TESTMODE1	AD3	
STRAP_TESTMODE2	AD4	
STRAP_UPSTRM_PORTSEL0	G24	
STRAP_UPSTRM_PORTSEL1	G25	
STRAP_UPSTRM_PORTSEL2	G26	
STRAP_STN0_PORTCFG0	AD24	
STRAP_STN0_PORTCFG1	AF24	
STRAP_STN1_PORTCFG0	C4	
STRAP_STN1_PORTCFG1	G1	
STRAP_RESERVED8	C23	
STRAP_RESERVED9	C26	
STRAP_PLL_BYPASS#	Y26	
STRAP_MGMT_PORT_EN	G2	
STRAP_SERDES_MODE_EN#	W26	
STRAP_I2C_SMBUS_EN	F2	
STRAP_I2C_SMBUS_CFG_EN#	W6	
I2C_ADDR0	E2	
STRAP_PROBE_MODE#	Y21	
STRAP_NT_UPSTRM_PORTSEL0	A2	
STRAP_NT_UPSTRM_PORTSEL1	G6	
STRAP_NT_UPSTRM_PORTSEL2	AA18	
STRAP_GEN1_GEN2	H24	
STRAP_RESERVED1	N6	
STRAP_RESERVED2	N21	
STRAP_RESERVED3	W3	
STRAP_RESERVED16	AE24	

R231 10k
R232

U42

AT25256B

PEX_EE_CSn
PEX_EE_DO
PEX_EE_SK
PEX_EE_DI

C637 10u
C341 0.1u
C340 0.1u

U28

TCA6416A

SHPC_INT#
PEX_MASTER_SDA
PEX_MASTER_SCL

P00	1	nSHP_PWRLED
P01	2	nSHP_ATNLED
P02	3	SHP_PWREN
P03	4	SHP_CLKEN
P04	5	SHP_PERST
P05	6	INTERLOCK
P06	7	
P07	8	
P10	10	
P11	11	
P12	12	
P13	13	
P14	14	nSHP_PRSNT
P15	15	nSHP_MRL
P16	16	nSHP_BUTTON
P17	17	

C689 10u
C628 0.1u

U31

POWER

PEX8732

PEX0P9V
PEX1P0VA
PEX1P8VA
SYS18

C262–C266, C241–C245

0.01u, 0.1u

C267–C271, C235–C239, C240

0.01u, 0.1u, 4.7u

C272–C276, C246–C250, C249

0.01u, 0.1u, 4.7u

C334–C330, C332–C328, C335–C331, C333–C329, C321–C320, C314

0.01u, 0.1u, 4.7u

C338–C334, C336–C332, C339–C335, C337–C333, C298–C296, C286–C306, C299–C297, C287–C307, C300–C298, C288–C308, C301–C299, C289–C309, C302–C300, C290–C310, C307–C305, C292–C312, C308–C306, C293–C313, C303–C311, C294–C314, C304–C312, C295–C315, C305–C313, C296–C316, C306–C314, C297–C317, C291–C315

0.01u, 0.1u, 4.7u

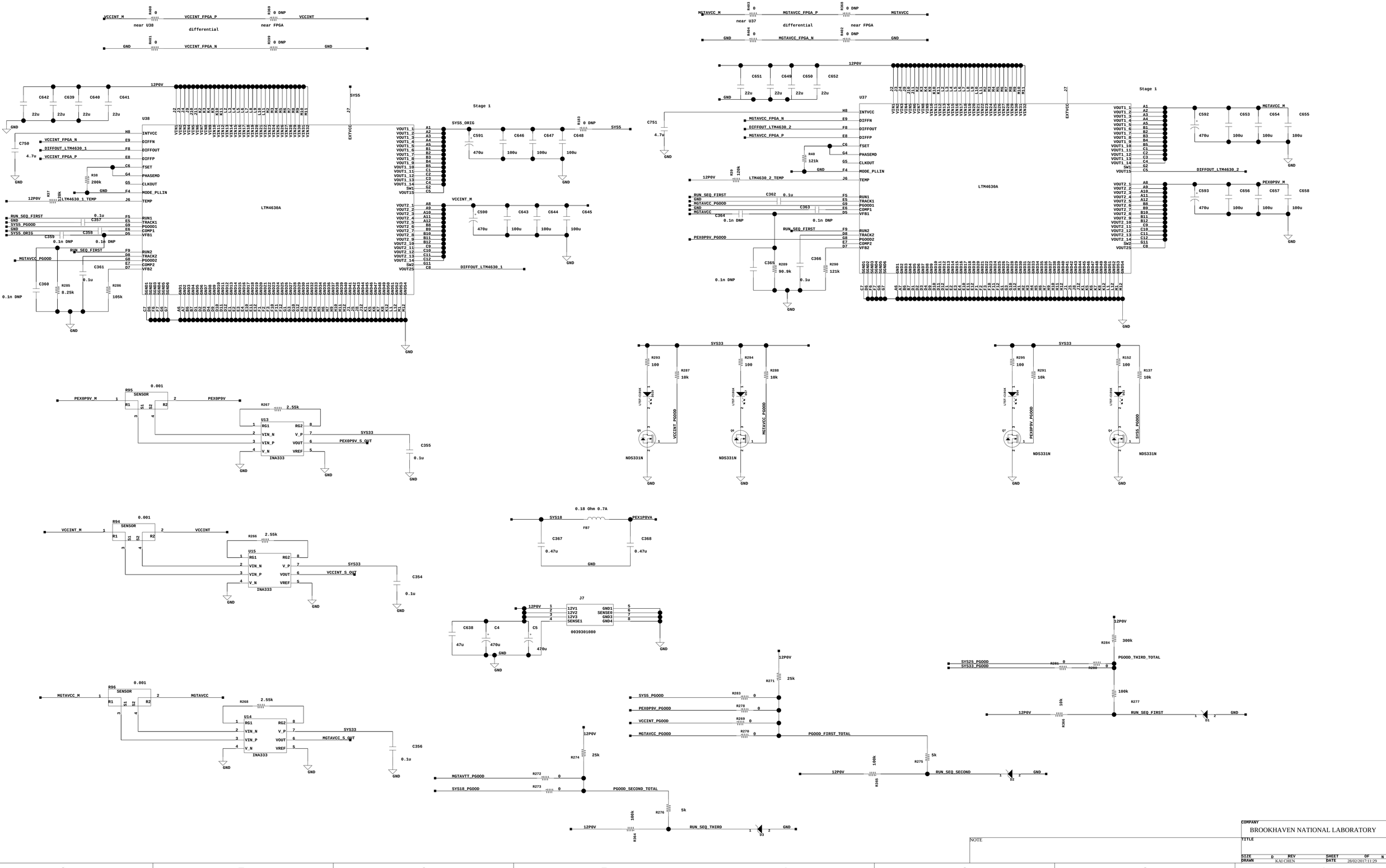
C275–C273, C250–C248, C276–C274, C251–C249, C277–C275, C252, C278–C276, C253–C251, C279–C277, C254–C252, C284–C282, C256–C254, C285–C283, C257–C255, C280–C278, C258–C256, C281–C279, C259–C257, C282–C280, C260–C258, C283–C281, C261–C259, C255

0.01u, 0.1u, 4.7u

C1 680u
C2 680u
C3 680u

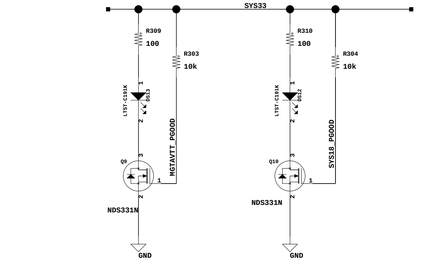
COMPANY	BROOKHAVEN NATIONAL LABORATORY
TITLE	PEX_PWR_CTRL
SIZE	D
REV	
SHEET	
OF	
N	
DRAWN	KAI CHEN
DATE	20/03/2017:21:27

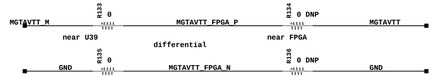
NOTE

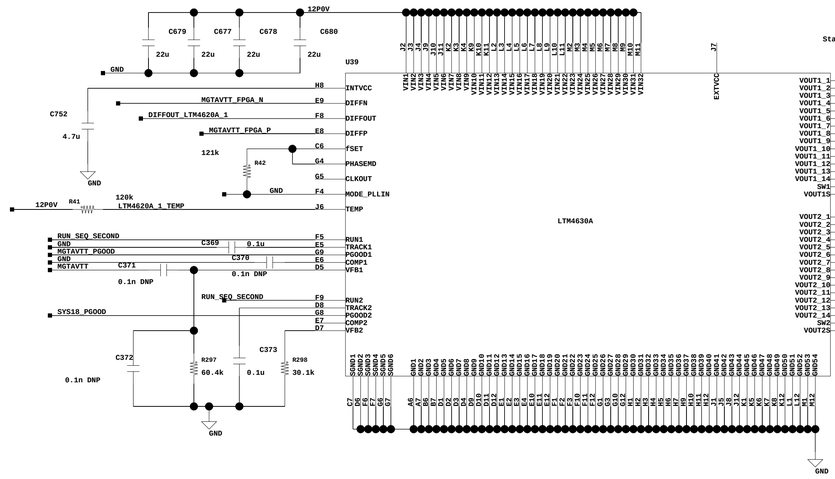


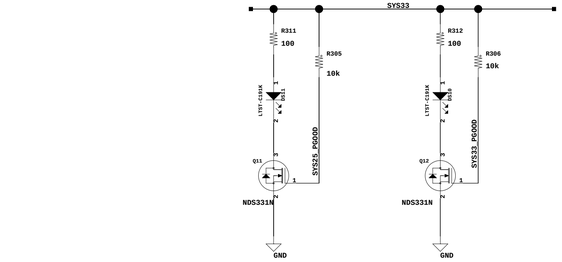
COMPANY	BROOKHAVEN NATIONAL LABORATORY						
TITLE							
SIZE	D	REV		SHEET		OF	N
DRAWN	KAI CHEN			DATE	28/02/2017 11:29		

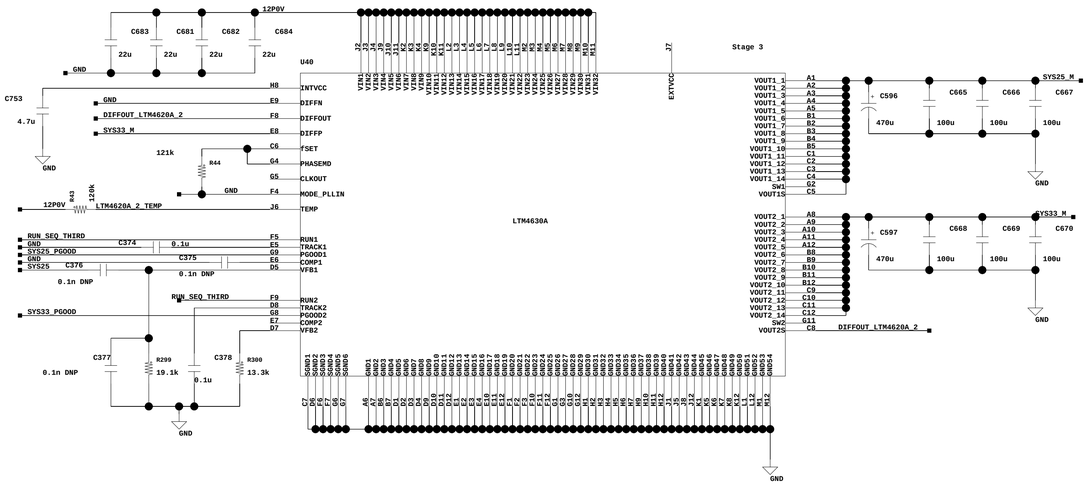
NOTE

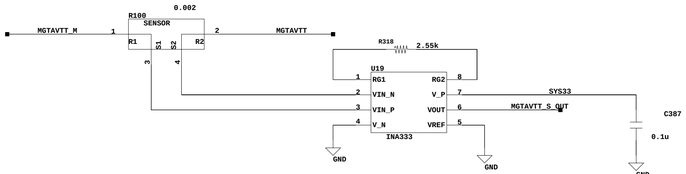


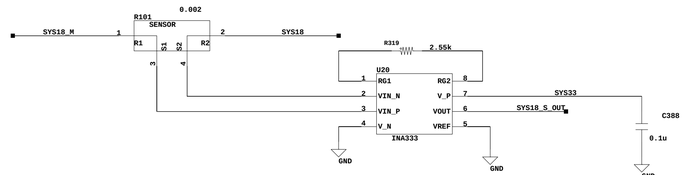


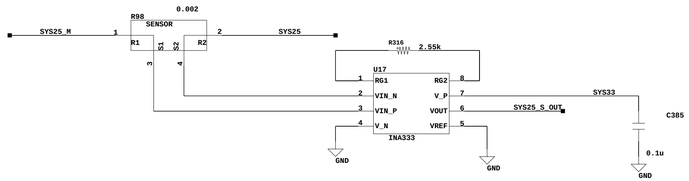


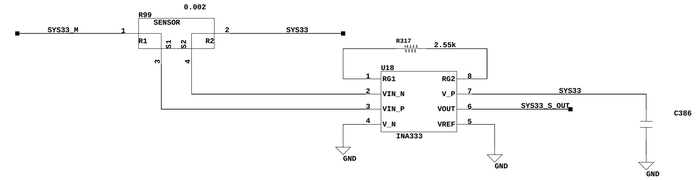






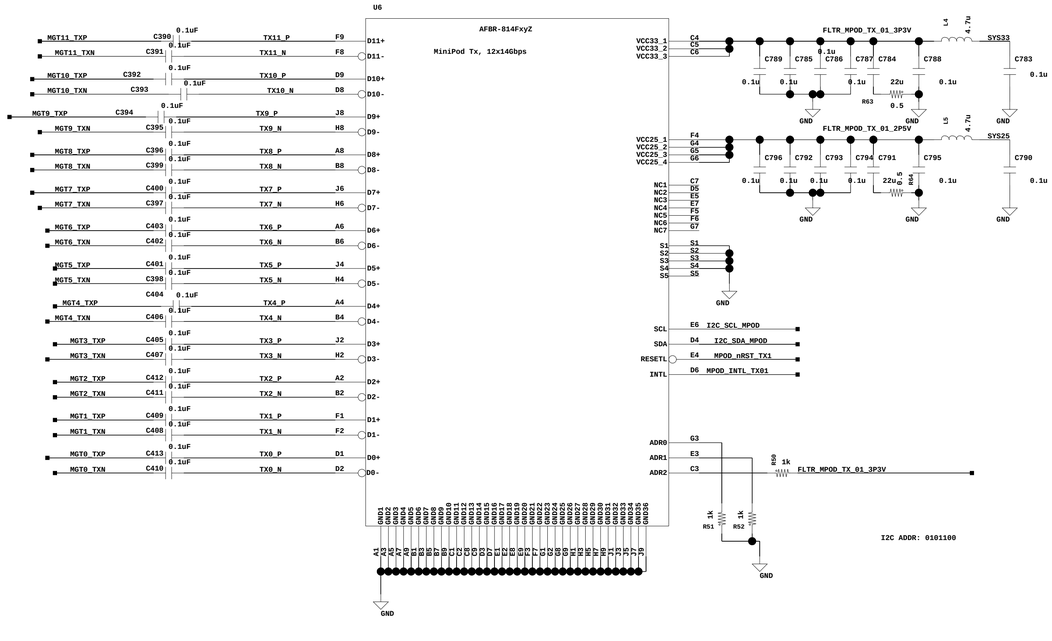


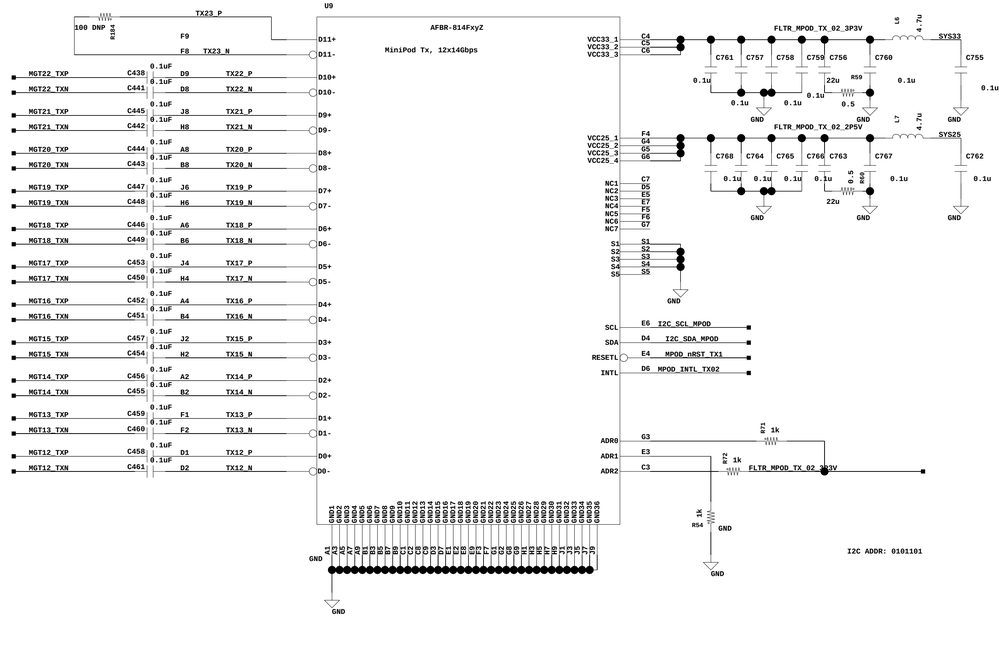


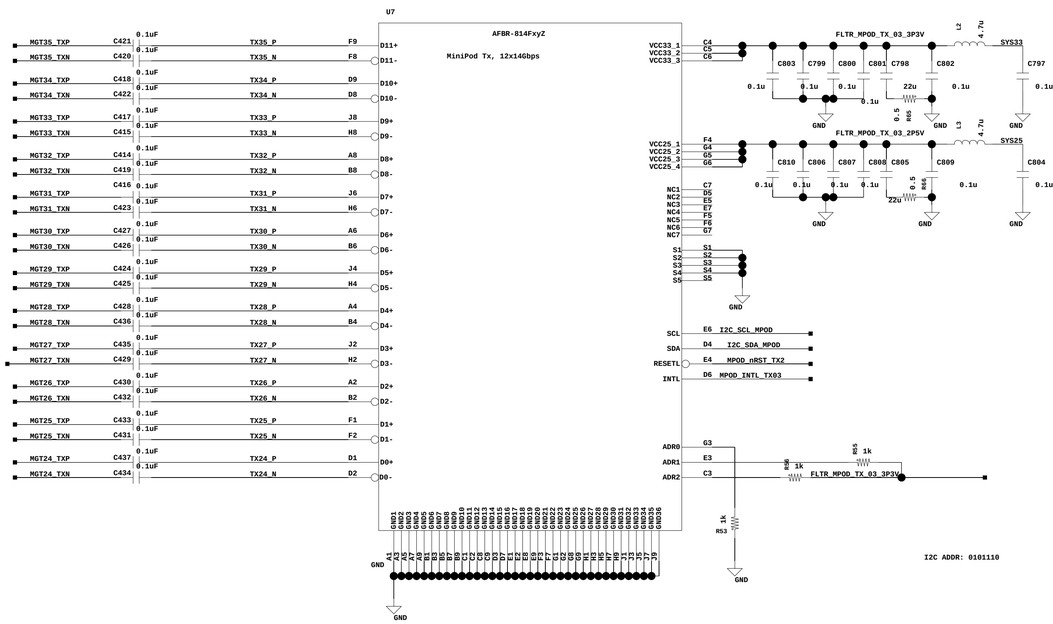


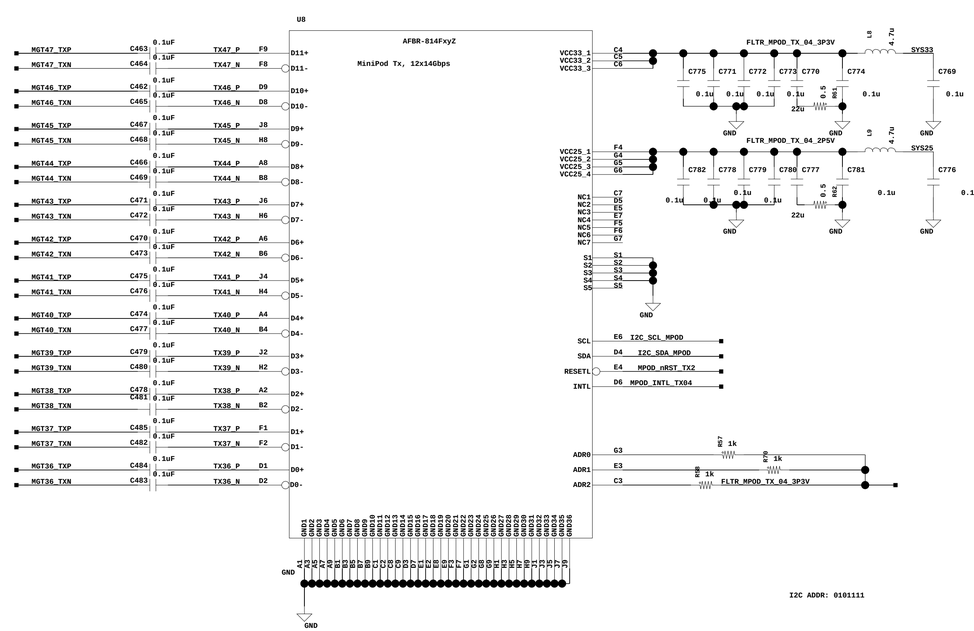
NOTE

COMPANY	BROOKHAVEN NATIONAL LABORATORY
TITLE	
SIZE D REV	SHEET OF N
DRAWN KAI CHEN	DATE 28/02/2017:11:29









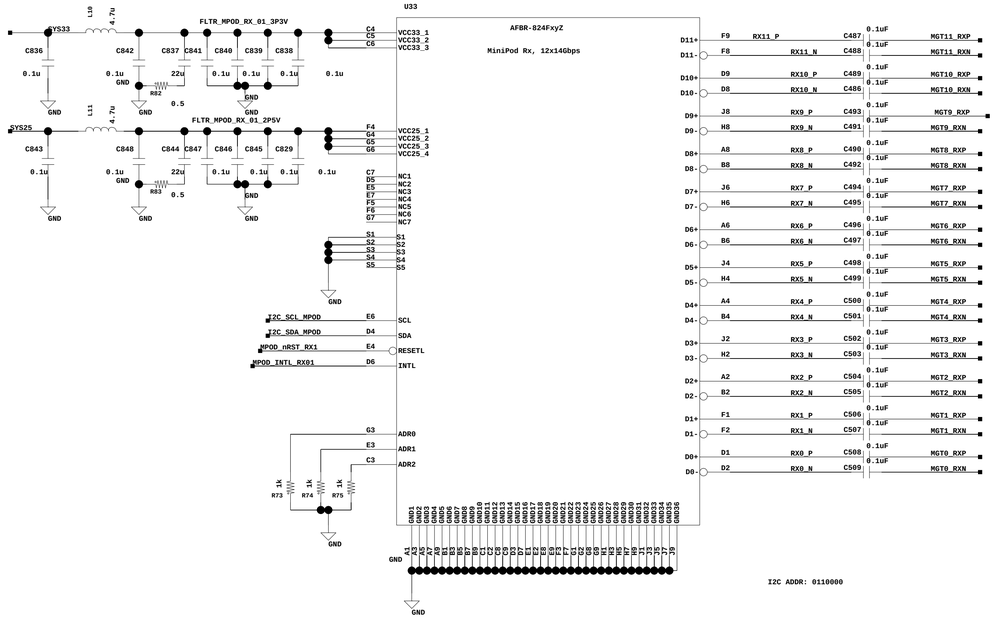
NOTE

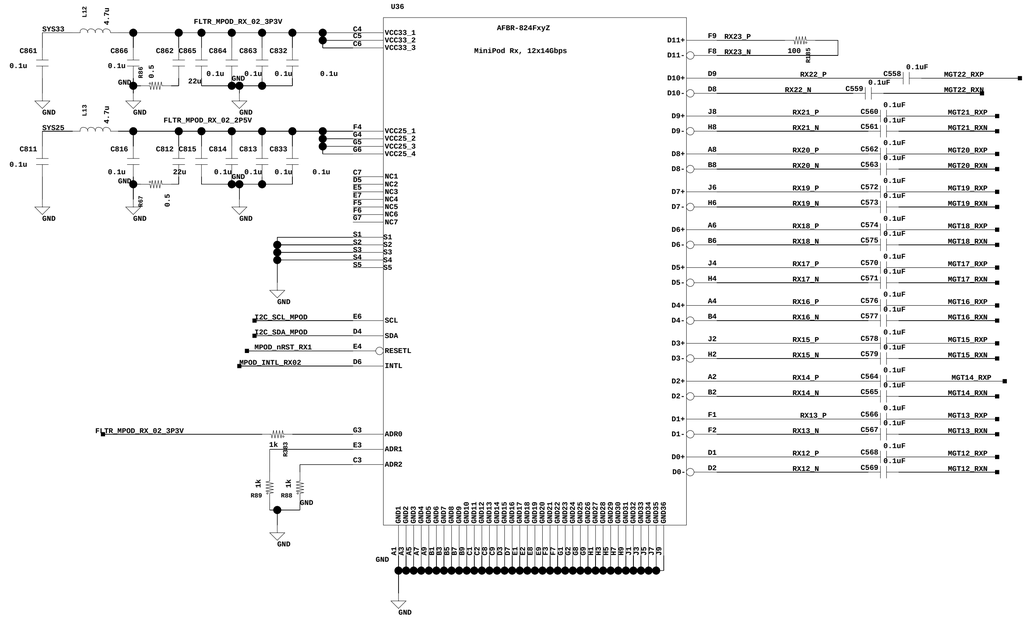
COMPANY BROOKHAVEN NATIONAL LABORATORY

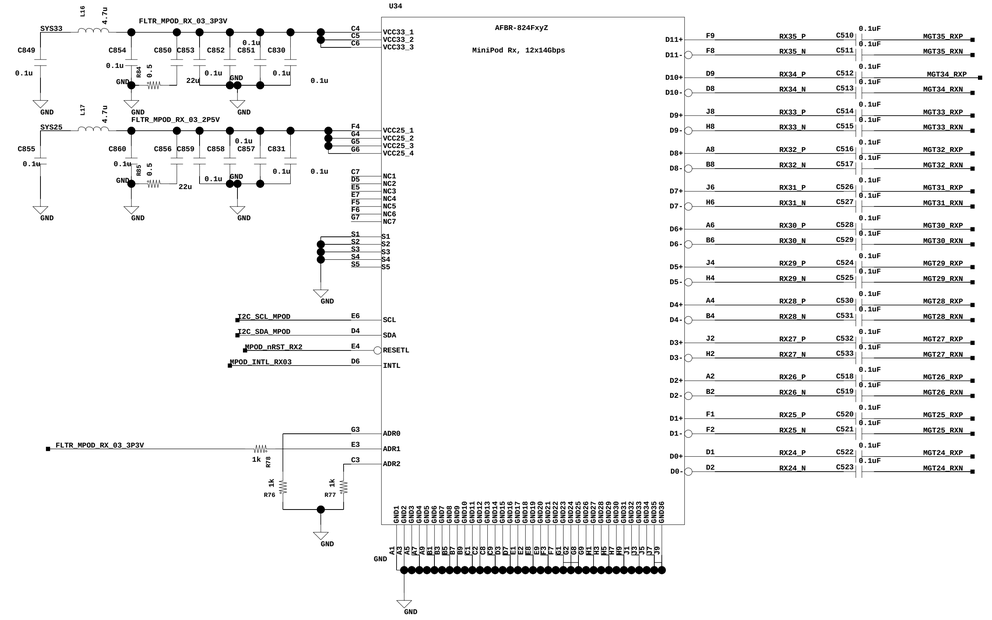
TITLE **MiniPOD TX**

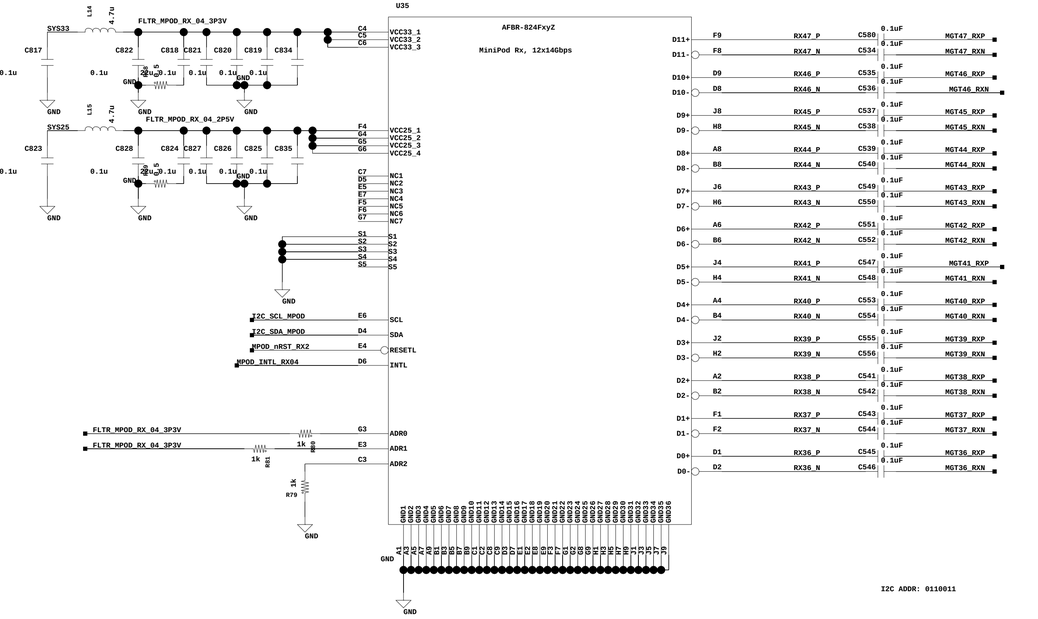
SIZE D REV SHEET OF N

DRAWN KAI CHEN DATE 21/03/2017 10:18









COMPANY	BROOKHAVEN NATIONAL LABORATORY
NOTE	
TITLE	PPOD RX
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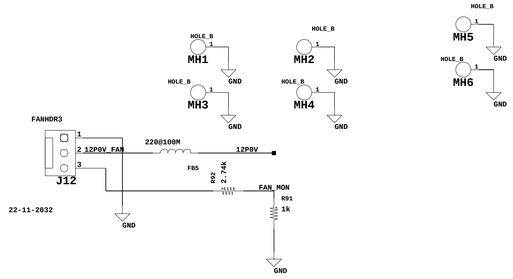
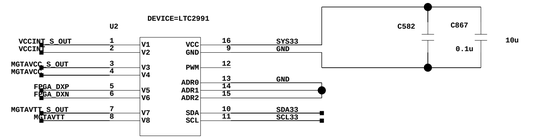
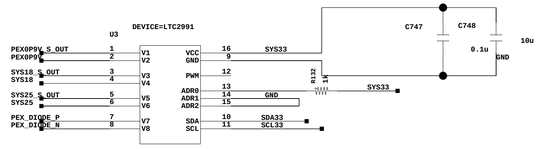
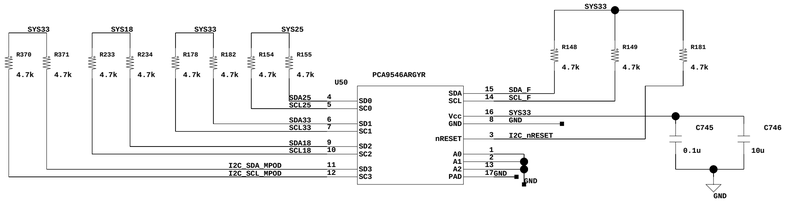
DRAWN	KAI CHEN
DATE	21/03/2017:10:19









NOTE

COMPANY	BROOKHAVEN NATIONAL LABORATORY
TITLE	
SIZE D REV	SHEET OF N
DRAWN KAI CHEN	DATE 20/03/2017 21:28